BSIMSOI3.1 MOSFET MODEL

Users' Manual

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How to get a copy of this manual and source code for the model:

`http://www-device.eecs.berkeley.edu/~bsimsoi`

Table of Contents

Chapter 1: Introduction

BSIMSOI is an international standard model for SOI (Silicon-On-Insulator) circuit design [20, 21]. This model is formulated on top of the BSIM3v3 framework [1]. It shares the same basic equations with the bulk model so that the physical nature and smoothness of BSIM3v3 are retained. Most parameters related to general MOSFET operation (non-SOI specific) are directly imported from BSIM3v3 to ensure parameter compatibility.

BSIMPD [18] is the Partial-Depletion (PD) mode of BSIMSOI. Many enhanced features are included in BSIMPD through the joint effort of the BSIM Team at UC Berkeley and IBM Semiconductor Research and Development Center (SRDC) at East Fishkill. In particular, the model has been tested extensively within IBM on its state-of-the-art high speed SOI technology.

BSIMPD, a derivative of BSIM3SOIv1.3 [2], has the following features and enhancements:

- Real floating body simulation in both I-V and C-V. The body potential is determined by the balance of all the body current components.
- An improved parasitic bipolar current model. This includes enhancements in the various diode leakage components, second order effects (high-level injection and Early effect), diffusion charge equation, and temperature dependence of the diode junction capacitance.
- An improved impact-ionization current model. The contribution from BJT current is also modeled by the parameter *Fbjtii*.
- A gate-to-body tunneling current model, which is important to thin-oxide SOI technologies.
- Enhancements in the threshold voltage and bulk charge formulation of the high positive body bias regime.
- Instance parameters (*Pdbcp, Psbcp, Agbcp, Aebcp, Nbc*) are provided to model the parasitics of devices with various body-contact and isolation structures [17].

- An external body node (the 6th node) and other improvements are introduced to facilitate the modeling of distributed body-resistance [17].
- Self heating. An external temperature node (the 7th node) is supported to facilitate the simulation of thermal coupling among neighboring devices.
- A unique SOI low frequency noise model, including a new excess noise resulting from the floating body effect [3].
- Width dependence of the body effect is modeled by parameters (*K1, K1w1, K1w2*).
- Improved history dependence of the body charges with two new parameters, (*Fbody, DLCB*).
- An instance parameter *Vbsusr* is provided for users to set the transient initial condition of the body potential.
- The new charge-thickness capacitance model introduced in BSIM3v3.2 [4], capMod=3, is included.

Chapter 2: MOS I-V Model

A typical PD SOI MOSFET structure is shown in Fig. 2.1. The device is formed on a thin SOI film of thickness T_{si} on top of a layer of buried oxide with thickness T_{box}. In the floating body configuration, there are four external biases which are gate voltage (V_g), drain voltage (V_d), source voltage (V_s) and substrate bias (V_e). The body potential (V_b) is iterated in circuit simulation. If a body contact is applied, there will be one more external bias, the body contact voltage (V_p).

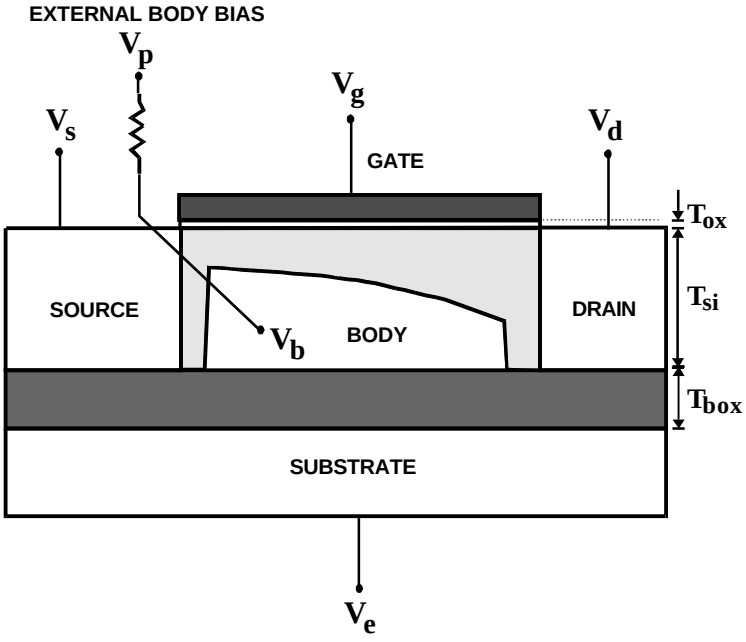


Fig. 2.1 Schematic of a typical PD SOI MOSFET.

Since the backgate (V_e) effect is decoupled by the neutral body, PD SOI MOSFETs have similar characteristics as bulk devices. Hence most PD SOI models reported [5, 6] were developed by adding some SOI specific effects onto a bulk model. These effects include parasitic bipolar current, self-heating and body contact resistance.

BSIMPD is formulated on top of the BSIM3v3 framework. In this way, a lot of physical effects which are common in bulk and SOI devices can be shared. These effects are reverse short channel effect, poly depletion, velocity saturation, DIBL in subthreshold and output resistance, short channel effect, mobility degradation, narrow width effect and source/drain series resistance [1, 4].

2.1. Floating Body Operation and Effective Body Potential

In BSIMPD, the floating body voltage is iterated by the SPICE engine. The result of iteration is determined by the body currents [7, 18]. In the case of DC, body currents include diode current, impact ionization, gate-induced drain leakage (GIDL), oxide tunneling and body contact current. For AC or transient simulations, the displacement currents originated from the capacitive coupling are also contributive.

To ensure a good model behavior during simulations, the iterated body potential V_{bs} is bounded by the following smoothing function

$$T_1 = V_{bsc} + 0.5\left[V_{bs} - V_{bsc} - d + \sqrt{(V_{bs} - V_{bsc} - d)^2 - 4dV_{bsc}}\right],\ V_{bsc} = -5V \tag{2.1}$$

$$V_{bsh} = f_{s1} - 0.5\left[f_{s1} - T_1 - d + \sqrt{(f_{s1} - T_1 - d)^2 + 4dT_1}\right],\ f_{s1} = 1.5V \tag{2.2}$$

Here the body potential V_{bsh} is equal to the V_{bs} bounded between (V_{bsc}, f_{s1}), and is used in the threshold voltage and bulk charge calculation. To validate the popular square root expression $\sqrt{f_s - V_{bsh}}$ in the MOSFET model, V_{bsh} is further limited to $0.95f_s$ to give the following effective body potential

$$V_{bseff} = f_{s0} - 0.5\left[f_{s0} - V_{bsh} - d + \sqrt{(f_{s0} - V_{bsh} - d)^2 + 4dV_{bsh}}\right],\ f_{s0} = 0.95f_s \tag{2.3}$$

2.2. Threshold Voltage in the High Vbs Regime

2.2.1. Linear Extrapolation for the Square-Root Epression

Using the V_{bseff} which is clamped to the surface potential f_s, the square-root dependence $\sqrt{f_s - V_{bseff}}$ of the threshold voltage is ensured to behave properly during simulations [20]. However the real body potential may be larger than the surface potential in state-of-the-art PD SOI technologies. To accurately count the body effect in such a high body bias regime, we extend the square-root expression by

$$sqrtPhisExt = \sqrt{f_s - V_{bseff}} + s\left(V_{bsh} - V_{bseff}\right), \quad s = -\frac{1}{2\sqrt{f_s - f_{s0}}} \tag{2.4}$$

where a linear extrapolation is employed for $V_{bsh} \geq 0.95 f_s$. Notice that $sqrtPhisExt = \sqrt{f_s - V_{bseff}}$ for $V_{bsh} \leq 0.95 f_s$.

2.2.2. Width Dependence of the Body Effect

In BSIMPD, the body effect coefficient K_1 is replaced by

$$K_{1eff} = K_1\left(1 + \frac{K_{1w1}}{W'_{eff} + K_{1w2}}\right) \tag{2.5}$$

to model the width dependence of the body effect. Notice that K_{1eff} approaches K_1 asymptotically as the effective channel width W'_{eff} increases. While the body effect coefficient will be determined by the parameters (K_{1w1}, K_{1w2}) when W'_{eff} becomes small so that the contribution from the channel-stop doping should be taken into account.

The complete equation of the threshold voltage V_{th} can be found in the Appendix C.

2.3. Bulk Charge Effect in the High Vbs Regime

The bulk charge factor in BSIMPD is modified from BSIM3v3 as

$$A_{bulk} = 1 + \left(\frac{K_{1eff}}{2\sqrt{(f_s + Ketas) - \frac{V_{bsh}}{1 + Keta \cdot V_{bsh}}}} \left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{T_{si} X_{dep}}} \left(1 - A_{gs} V_{gsteff} \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{T_{si} X_{dep}}} \right)^2 \right) + \frac{B_0}{W_{eff}' + B_1} \right) \right) \quad (2.6)$$

to accommodate the model behavior in the high body bias regime, which is important in PD SOI. The parameter *Ketas* acts like an effective increment of the surface potential, which can be used to adjust the A_{bulk} rollup with the body potential V_{bsh}. While the other parameter *Keta* is used to tune the rate of rollup with V_{bsh}. By using this new expression, the non-physical drain current roll-off due to the dramatic A_{bulk} rollup at high body bias can be avoided [20].

2.4. Single Drain Current Equation

After improving the V_{th} and A_{bulk} behavior in the high body bias regime, we can describe the MOSFET drain current by the same equation as BSIM3v3. The effective drain voltage V_{dseff} and effective gate overdrive voltage V_{gsteff} introduced in BSIM3v3 [1] are employed to link subthreshold, linear and saturation operation regions into a single expression as

$$I_{ds,MOSFET} = \frac{I_{ds0}}{1 + \frac{R_{ds} I_{dso}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)$$

$$b = m_{eff} C_{ox} \frac{W_{eff}}{L_{eff}}$$

$$I_{dso} = \frac{b V_{gsteff} \left(1 - A_{bulk} \frac{V_{dseff}}{2\left(V_{gsteff} + 2v_t\right)}\right) V_{dseff}}{1 + \frac{V_{dseff}}{E_{sat} L_{eff}}} \quad (2.7)$$

where R_{ds} is the source/drain series resistance, m_{eff} is the mobility, E_{sat} is the critical electrical field at which the carrier velocity becomes saturated and V_A accounts for channel length modulation (CLM) and DIBL as in BSIM3v3. The substrate current body effect (SCBE) [8, 9] on V_A is not included because it has been taken into account explicitly by the real floating body simulation determined by the body currents, which will be detailed in the next chapter.

Chapter 3: Body Currents Model

Body currents determine the body potential and therefore the drain current through the body effect. Beside the impact ionization current considered in BSIM3v3, diode (bipolar) current, GIDL, oxide tunneling and body contact current are all included in the BSIMPD model [Fig. 3.1] to give an accurate body-potential prediction in the floating body simulation [18].

3.1. Diode and Parasitic BJT Currents

In this section we describe various current components originated from **B**ody-to-**S**ource/**D**rain (B-S/D) injection, recombination in the B-S/D junction depletion region, **S**ource/**D**rain-to-**B**ody (S/D-B) injection, recombination current in the neutral body, and diode tunneling current.

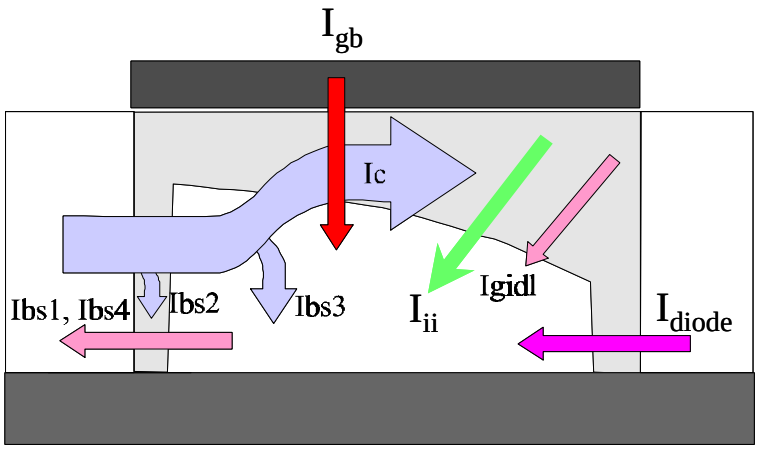


Fig. 3.1 Various current components inside the body.

The backward injection current in the B-S/D diode can be expressed as

$$I_{bs1} = W_{dios} T_{si} j_{sdif} \left(\exp\left(\frac{V_{bs}}{n_{dio} V_t} \right) - 1 \right)$$
$$I_{bd1} = W_{diod} T_{si} j_{sdif} \left(\exp\left(\frac{V_{bd}}{n_{dio} V_t} \right) - 1 \right) \quad (3.1)$$

Here $n_{dio}, j_{sdif}, W_{dios}, W_{diod}$ are the non-ideality factor, the saturation current, the effective B-S diode width and the B-D diode width, respectively.

The carrier recombination and trap-assisted tunneling current in the space-charge region is modeled by

$$I_{bs2} = W_{dios} T_{si} j_{srec} \left(\exp\left(\frac{V_{bs}}{0.026 n_{recf}} \right) - \exp\left(\frac{V_{sb}}{0.026 n_{recr}} \frac{V_{rec0}}{V_{rec0} + V_{sb}} \right) \right)$$
$$I_{bd2} = W_{diod} T_{si} j_{srec} \left(\exp\left(\frac{V_{bd}}{0.026 n_{recf}} \right) - \exp\left(\frac{V_{db}}{0.026 n_{recr}} \frac{V_{rec0}}{V_{rec0} + V_{db}} \right) \right) \quad (3.2)$$

Here $n_{recf}, n_{recr}, j_{srec}$ are non-ideality factors for forward bias and reverse bias, the saturation current, respectively. Note that the parameter V_{rec0} is provided to model the current roll-off in the high reverse bias regime.

The reverse bias tunneling current, which may be significant in junctions with high doping concentration, can be expressed as

$$\boldsymbol{I_{bs4} = W_{dios} T_{si} j_{stun} \left(1 - exp\left(\frac{V_{sb}}{0.026 n_{tun}} \frac{V_{tun0}}{V_{tun0} + V_{sb}} \right) \right)}$$
$$\boldsymbol{I_{bd4} = W_{diod} T_{si} j_{stun} \left(1 - exp\left(\frac{V_{db}}{0.026 n_{tun}} \frac{V_{tun0}}{V_{tun0} + V_{db}} \right) \right)} \quad (3.3)$$

where j_{stun} is the saturation current. The parameters n_{tun} and V_{tun0} are provided to better fit the data.

The recombination current in the neutral body can be described by

$$
\begin{aligned}
I_{bs3} &= (1-a_{bjt})I_{en}\left[\exp\left(\frac{V_{bs}}{n_{dio}V_t}\right)-1\right]\frac{1}{\sqrt{E_{hlis}+1}} \\
I_{bd3} &= (1-a_{bjt})I_{en}\left[\exp\left(\frac{V_{bd}}{n_{dio}V_t}\right)-1\right]\frac{1}{\sqrt{E_{hlid}+1}} \\
I_{en} &= W'_{eff}T_{si}j_{sbjt}\left[L_{bjt0}\left(\frac{1}{L_{eff}}+\frac{1}{L_n}\right)\right]^{N_{bjt}} \\
E_{hlis} &= A_{hli\_eff}\left[\exp\left(\frac{V_{bs}}{n_{dio}V_t}\right)-1\right] \\
E_{hlid} &= A_{hli\_eff}\left[\exp\left(\frac{V_{bd}}{n_{dio}V_t}\right)-1\right] \\
a_{bjt} &= \exp\left[-0.5\left(\frac{L_{eff}}{L_n}\right)^2\right]
\end{aligned}
\tag{3.4}
$$

Here a_{bjt} is the bipolar transport factor, whose value depends on the ratio of the effective channel length L_{eff} and the minority carrier diffusion length L_n. j_{sbjt} is the saturation current, while the parameters L_{bjt0} and N_{bjt} are provided to better fit the forward injection characteristics. Notice that E_{hlis} and E_{hlid}, determined by the parameter A_{hli}, stand for the high level injection effect in the B-S/D diode, respectively.

The parasitic bipolar transistor current is important in transient body discharge, especially in pass-gate floating body SOI designs [7]. The BJT collector current is modeled as

$$
\begin{aligned}
I_c &= a_{bjt}I_{en}\left\{\exp\left[\frac{V_{bs}}{n_{dio}V_t}\right]-\exp\left[\frac{V_{bd}}{n_{dio}V_t}\right]\right\}\frac{1}{E_{2nd}} \\
E_{2nd} &= \frac{E_{ely}+\sqrt{E_{ely}{}^2+4E_{hli}}}{2} \\
E_{ely} &= 1+\frac{V_{bs}+V_{bd}}{V_{Abjt}+A_{ely}L_{eff}} \\
E_{hli} &= E_{hlis}+E_{hlid}
\end{aligned}
\tag{3.5}
$$

where E_{2nd} is composed of the Early effect E_{ely} and the high level injection roll-off E_{hli}. Note that $E_{2nd} \to E_{ely}$ as $E_{ely} >> E_{hli}$. While $E_{2nd} \to \sqrt{E_{hli}}$ as $E_{hli} >> E_{ely}$, in which case the Early voltage $V_{Abjt} + A_{ely}L_{eff}$ is high.

To sum up, the total B-S current is $I_{bs} = \sum_{i=1}^{4} I_{bsi}$, and the total B-D current is $I_{bd} = \sum_{i=1}^{4} I_{bdi}$. The total drain current including the BJT component can then be expressed as

$$I_{ds,total} = I_{ds,MOSFET} + I_c \tag{3.6}$$

3.2. New Impact Ionization Current Equation

An accurate impact ionization current equation is crucial to the PD SOI model since it may affect the transistor output characteristics through the body effect [11]. Hence in BSIMPD we use a more decent expression [22] to formulate the impact ionization current I_{ii} as

$$\begin{aligned}
I_{ii} &= a_0(I_{ds,MOSFET} + F_{bjtii}I_c)\exp\left(\frac{V_{diff}}{b_2 + b_1V_{diff} + b_0V_{diff}^{\ 2}}\right) \\
V_{diff} &= V_{ds} - V_{dsatii} \\
V_{dsatii} &= VgsStep + \left[V_{dsatii0}\left(1 + T_{ii}\left(\frac{T}{T_{nom}} - 1\right)\right) - \frac{L_{ii}}{L_{eff}}\right] \\
VgsStep &= \left(\frac{E_{satii}L_{eff}}{1 + E_{satii}L_{eff}}\right)\left(\frac{1}{1 + S_{ii1}V_{gsteff}} + S_{ii2}\right)\left(\frac{S_{ii0}V_{gst}}{1 + S_{iid}V_{ds}}\right)
\end{aligned} \tag{3.7}$$

Here the $F_{bjtii}I_c$ term represents the contribution from the parasitic bipolar current. Notice that the classical impact ionization current model [12] adopted in BSIM3v3 is actually a special case of Eqn. (3.6) when $(b_0, b_1, b_2) = (-1,0,0)$. However, the dependence of $\log(I_{ii}/I_{ds})$ on the drain overdrive voltage V_{diff} is quite linear [22] for state-of-the-art SOI technologies due to thermally assisted impact ionization [23]. In this case, $(b_0, b_1, b_2) \cong (0,0,1)$.

The extracted saturation drain voltage V_{dsatii} depends on the gate overdrive voltage V_{gst} and L_{eff}. One can first extract the parameters $(V_{dsatii0}, L_{ii})$ by the V_{dsatii} - L_{eff} characteristics at $V_{gst} = 0$. All the other parameters $(E_{satii}, S_{ii1}, S_{ii2}, S_{ii0}, S_{iid})$ can then be determined by the plot of V_{dsatii} versus V_{gs} for different L_{eff}. Notice that a linear temperature dependence of $V_{dsatii0}$ with the parameter T_{ii} is also included.

3.3. Gate Induced Drain Leakage Current

GIDL can be important in PD SOI because it can affect the body potential in the low V_{gs} and high V_{ds} regime. The formula for GIDL current is:

$$I_{dgidl} = a_{gidl} \cdot E_s \cdot \exp\left(-\frac{b_{gidl}}{E_s}\right),\ E_s = \frac{V_{ds} - V_{gs} - c}{3 \cdot T_{ox}} \tag{3.8}$$

Here χ is the fitting parameter with a default value 1.2, which is the correct value for uniformly doped substrates with no LDD or fully overlapped LDD. However, in general χ can be different from 1.2, depending on the doping profile at the drain edge [13]. For the sake of symmetry, GIDL current is accounted for both at the drain and source side (I_{sgidl}).

3.4. Oxide Tunneling Current

For thin oxide (below 20Å), oxide tunneling is important in the determination of floatin-body potential [20]. In BSIMPD the following equations are used to calculate the tunneling current density J_{gb}:

In inversion,

$$
\begin{aligned}
J_{gb} &= A\frac{V_{gb}V_{aux}}{T_{ox}^2}\left(\frac{\mathrm{T_{oxref}}}{T_{oxqm}}\right)^{\mathrm{N_{tox}}} exp\left(\frac{-B\left(\acute{a}_{\mathrm{gb1}}-\hat{a}_{\mathrm{gb1}}\left|V_{ox}\right|\right)T_{ox}}{1-\left|V_{ox}\right|/\mathrm{V_{gb1}}}\right)\\
V_{aux} &= \mathrm{V_{EVB}}\,ln\left(1+exp\left(\frac{\left|V_{ox}\right|-\ddot{O}_{\mathrm{g}}}{\mathrm{V_{EVB}}}\right)\right)\\
A &= \frac{q^3}{8phf_b}\\
B &= \frac{8p\sqrt{2m_{ox}}f_b^{3/2}}{3hq}\\
f_b &= 4.2eV\\
m_{ox} &= 0.3m_0
\end{aligned}
\qquad (3.9)
$$

In accumulation,

$$
\begin{aligned}
J_{gb} &= A\frac{V_{gb}V_{aux}}{T_{ox}^2}\left(\frac{\mathrm{T_{oxref}}}{T_{oxqm}}\right)^{\mathrm{N_{tox}}} exp\left(\frac{-B\left(\acute{a}_{\mathrm{gb2}}-\hat{a}_{\mathrm{gb2}}\left|V_{ox}\right|\right)T_{ox}}{1-\left|V_{ox}\right|/\mathrm{V_{gb2}}}\right)\\
V_{aux} &= \mathrm{V_{ECB}}V_t\,ln\left(1+exp\left(-\frac{V_{gb}-V_{fb}}{\mathrm{V_{ECB}}}\right)\right)\\
A &= \frac{q^3}{8phf_b}\\
B &= \frac{8p\sqrt{2m_{ox}}f_b^{3/2}}{3hq}\\
f_b &= 3.1eV\\
m_{ox} &= 0.4m_0
\end{aligned}
\qquad (3.10)
$$

Please see Appendix B for model parameter descriptions.

3.5. Body Contact Current

In BSIMPD, a body resistor is connected between the body (B node) and the body contact (P node) if the transistor has a body-tie. The body resistance is modeled by

$$
R_{bp} = \left(R_{body}\frac{W'_{eff}}{L_{eff}}\right)\left\|\left(R_{halo}\frac{W'_{eff}}{2}\right),\right. \quad R_{bodyext} = R_{bsh}N_{rb} \qquad (3.11)
$$

Here R_{bp} and $R_{bodyext}$ represent the intrinsic and extrinsic body resistance respectively. R_{body} is the intrinsic body sheet resistance, R_{halo} accounts for the effect of halo implant, N_{rb} is the number of square from the body contact to the device edge and R_{bsh} is the sheet resistance of the body contact diffusion.

The body contact current I_{bp} is defined as the current flowing through the body resistor:

$$I_{bp} = \frac{V_{bp}}{R_{bp} + R_{bodyext}} \tag{3.12}$$

where V_{bp} is the voltage across the B node and P node. Notice that $I_{bp} = 0$ if the transistor has a floating body.

3.6. Body Contact Parasitics [17]

The effective channel width may change due to the body contact. Hence the following equations are used:

$$\begin{aligned} W_{eff} &= W_{drawn} - N_{bc} dW_{bc} - (2 - N_{bc}) dW \\ W_{eff}' &= W_{drawn} - N_{bc} dW_{bc} - (2 - N_{bc}) dW' \\ W_{diod} &= W_{eff}' + P_{dbcp} \\ W_{dios} &= W_{eff}' + P_{sbcp} \end{aligned} \tag{3.13}$$

Here dW_{bc} is the width offset for the body contact isolation edge. N_{bc} is the number of body contact isolation edge. For example: $N_{bc} = 0$ for floating body devices, $N_{bc} = 1$ for T-gate structures and $N_{bc} = 2$ for H-gate structures. P_{dbcp} / P_{sbcp} represents the parasitic perimeter length for body contact at drain/source side. The body contact parasitics may affect the I-V significantly for narrow width devices [20].

After introducing all the mechanisms that contribute the body current, we can express the nodal equation (KCL) for the body node as

$$(I_{bs} + I_{bd}) + I_{bp} - I_{ii} - (I_{dgidl} + I_{sgidl}) - I_{gb} = 0 \tag{3.14}$$

Eqn. (3.14) is important since it determines the body potential through the balance of various body current components. The I-V characteristics can then be correctly predicted after this critical body potential can be well anchored.

Chapter 4: MOS C-V Model

BSIMPD approaches capacitance modeling by adding SOI-specific capacitive effect to the C-V model of BSIM3v3. Similar to the I-V case, the body charges belonged to the floating body node will be our emphasis. The model incorporates features listed below with the SOI-specific features bold-faced and italicized.

- Separate effective channel length and width for IV and CV models.
- The CV model is not piece-wise (i.e. divided into inversion, depletion, and accumulation). Instead, a single equation is used for each nodal charge covering all regions of operation. This ensures continuity of all derivatives and enhances convergence properties. Just like in BSIM3v3, the inversion and body capacitances are continuous at the threshold voltage.
- Threshold voltage formulation is consistent with the IV model. Body effect and DIBL are automatically incorporated in the capacitance model.
- Intrinsic capacitance model has two options. The capMod = 2 option yields capacitance model based on BSIM3v3 short channel capacitance model. The capMod = 3 option is the new charge-thickness model from BSIM3v3.2 [4].
- Front gate overlap capacitance is comprised of two parts: 1) a bias independent part which models the effective overlap capacitance between the gate and the heavily doped source/drain, and 2) a gate bias dependent part between the gate and the LDD region.
- Bias independent fringing capacitances are added between the gate and source as well as the gate and drain. ***A sidewall source/drain to substrate (under the buried oxide) fringing capacitance is added.***
- ***A source/drain-buried oxide-Si substrate parasitic MOS capacitor is added.***
- ***Body-to-back-gate coupling is added.***

A good intrinsic charge model is important in bulk MOSFETs because intrinsic capacitance comprises a sizable portion of the overall capacitance, and because a well behaved charge model is required for robust large circuit simulation convergence. In analog applications there are devices biased near the threshold voltage. Thus, a good charge model must be well-behaved in transition regions as well. To ensure proper behavior, both the I-V and C-V model equations should be developed from an identical set of charge equations so that C_{ij}/I_d is well behaved.

A good physical charge model of SOI MOSFETs is even more important than in bulk. This is because transient behavior of the floating body depends on capacitive currents [18]. Also, due to the floating body node, convergence issues in PD SOI are more volatile than in bulk, so that charge smoothness and robustness are important. An example is that a large negative guess of body potential by SPICE during iterations can force the transistor into depletion, and a smooth transition between depletion and inversion is required. Therefore the gate/source/drain/backgate to body capacitive coupling is important in PD SOI.

4.1. Charge Conservation

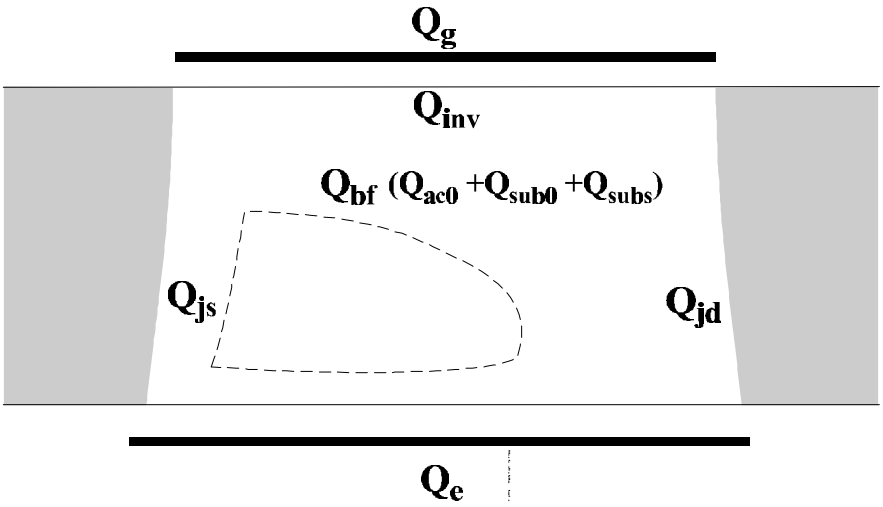


Fig. 4.1 Intrinsic charge components in BSIMPD CV model

To ensure charge conservation, terminal charges instead of terminal voltages are used as state variables. The terminal charges Q_g, Q_d, Q_s, Q_b, and Q_e are the charges associated with the **g**ate, **d**rain, **s**ource, **b**ody, and substrat**e** respectively. These charges can be expressed in terms of inversion charge (Q_{inv}), front gate body charge (Q_{Bf}), source junction charge (Q_{js}) and drain junction charge (Q_{jd}). The intrinsic charges are distributed between the nodes as shown in Fig. 4.1. The charge conservation equations are:

$$\begin{aligned}
Q_{Bf} &= Q_{ac0} + Q_{sub0} + Q_{subs} \\
Q_{inv} &= Q_{inv,s} + Q_{inv,d} \\
Q_g &= -\left(Q_{inv} + Q_{Bf}\right) \\
Q_b &= Q_{Bf} - Q_e + Q_{js} + Q_{jd} \\
Q_s &= Q_{inv,s} - Q_{js} \\
Q_d &= Q_{inv,d} - Q_{jd} \\
Q_g + Q_e + Q_b + Q_s + Q_d &= 0
\end{aligned} \tag{4.1}$$

The front gate body charge (Q_{Bf}) is composed of the accumulation charge (Q_{ac0}) and the bulk charge (Q_{sub0} and Q_{subs}), which may be divided further into two components: the bulk charge at V_{ds}=0 (Q_{sub0}), and the bulk charge induced by the drain bias (Q_{subs}) (similar to δQ_{sub} in BSIM3v3).

All capacitances are derived from the charges to ensure charge conservation. Since there are 5 charge nodes, there are 25 (as compared to 16 in BSIM3v3) components. For each component: $C_{ij} = \frac{dQ_i}{dV_j}$, where *i* and *j* denote transistor nodes. In addition, $\sum_i C_{ij} = \sum_j C_{ij} = 0$.

4.2. Intrinsic Charges

BSIMPD uses similar expressions to BSIM3v3 for Q_{inv} and Q_{Bf}. First, the bulk charge constant A_{bulkCV} is defined as

$$A_{bulkCV} = A_{bulk0}\left(1+\left(\frac{CLC}{L_{active}}\right)^{CLE}\right) \tag{4.2}$$

where

$$A_{bulk0} = A_{bulk}\left(V_{gsteff}=0\right) \tag{4.3}$$

This is done in order to empirically fit V_{dsatCV} to channel length. Experimentally,

$$V_{dsatIV} < V_{dsatCV} < V_{dsatIV}\big|_{L\to\infty} = \frac{V_{gsteffCV}}{A_{bulk}} \tag{4.4}$$

The effective CV V_{gst} is defined as

$$V_{gsteffCV} = nv_t \ln\left(1+\exp\left[\frac{V_{gs}-V_{th}}{nv_t}\right]\right) \tag{4.5}$$

Then we can calculate the CV saturation drain voltage

$$V_{dsatCV} = V_{gsteffCV} \,/\, A_{bulkCV}\,. \tag{4.6}$$

Define effective CV V_{ds} as

$$V_{dsCV} = V_{dsatCV} - \frac{1}{2}(V_{dsatCV} - V_{ds} - d + \sqrt{(V_{dsatCV} - V_{ds} - d)^2 + 4dV_{dsatCV}}) \tag{4.7}$$

Then the inversion charge can be expressed as

$$Q_{inv} = -W_{active}L_{active}C_{ox}\left(\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{dsCV}\right) + \frac{A_{bulkCV}{}^2 V_{dsCV}{}^2}{12\left(V_{gsteffCV} - \frac{A_{bulkCV}{}^2}{2}V_{dsCV}\right)}\right) \tag{4.8}$$

where W_{active} and L_{active} are the effective channel width and length in CV, respectively. The channel partition can be set by the *Xpart* parameter. The exact evaluation of source and drain charges for each partition option is presented in Appendix C.

A parameter V_{FBeff} is used to smooth the transition between accumulation and depletion regions. The expression for V_{FBeff} is:

$$V_{FBeff} = V_{fb} - 0.5\left[\left(V_{fb} - V_{gb} - d\right) + \sqrt{\left(V_{fb} - V_{gb} - d\right)^2 + d^2}\right] \tag{4.9}$$

where $V_{gb} = V_{gs} - V_{bseff}$, $V_{fb} = V_{th} - f_s - K_{1eff}\sqrt{f_s - V_{bseff}}$.

The physical meaning of the function is the following: it is equal to V_{gb} for $V_{gb}<V_{FB}$, and equal to V_{FB} for $V_{gb}>V_{FB}$. Using V_{FBeff}, the accumulation charge can be calculated as

$$Q_{ac0} = -F_{body} W_{active} L_{activeB} C_{ox} (V_{FBeff} - V_{fb}) \tag{4.10}$$

where $L_{activeB} = L_{active} - DLCB$. Notice that the parameters F_{body} and $DLCB$ are provided to give a better fit for the SOI-specific history dependence of the body charge [14].

The gate-induced depletion charge and drain-induced depletion charge can be expressed as

$$Q_{sub0} = -F_{body} W_{active} L_{activeB} C_{ox} \frac{{K_{1eff}}^2}{2}\left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FBeff} - V_{gsteffCV} - V_{bseff})}{{K_{1eff}}^2}}\right) \tag{4.11}$$

$$Q_{subs} = F_{body} W_{active} L_{activeB} K_{1eff} C_{ox} \left(1 - A_{bulkCV}\right)\left[\frac{V_{dsCV}}{2} - \frac{A_{bulkCV} V_{dsCV}^2}{12\left(V_{gsteffCV} - A_{bulkCV} V_{dsCV}/2\right)}\right] \tag{4.12}$$

respectively.

Finally, the back gate body charge can be modeled by

$$Q_e = F_{body} W_{active} L_{activeBG} C_{box} \left(V_{es} - V_{fbb} - V_{bseff}\right) \tag{4.13}$$

where $L_{activeBG} = L_{activeB} + 2dL_{bg}$. The parameter dL_{bg} is provided to count the difference of $L_{activeB}$ and $L_{activeBG}$ due to the source/drain extension in the front channel.

For capMod=3, the flat band voltage is calculated from the bias-independent threshold voltage, which is different from capMod=2. For the finite thickness formulation, refer to Chapter 4 of BSIM3v3.2 Users' Manual.

4.3. Source/Drain Junction Charges

Beside the junction depletion capacitance considered in BSIM3v3, the diffusion capacitance, which is important in the forward body-bias regime [20], is also included in BSIMPD. The source/drain junction charges Q_{jswg} / Q_{jdwg} can therefore be expressed as

$$\begin{aligned} Q_{jswg} &= Q_{bsdep} + Q_{bsdif} \\ Q_{jdwg} &= Q_{bddep} + Q_{bddif} \end{aligned} \tag{4.14}$$

The depletion charges Q_{bsdep} / Q_{bddep} have similar expressions as in BSIM3v3 [Appendix C]. While the diffusion charges Q_{bsdif} / Q_{bddif} can be modeled by

$$\begin{aligned} Q_{bsdif} &= tW_{eff}{}'T_{si}J_{sbjt}\left[1+L_{dif0}\left(L_{bjt0}\left(\frac{1}{L_{eff}}+\frac{1}{L_n}\right)^{N_{dif}}\right)\right]\left[\exp\left(\frac{V_{bs}}{n_{dio}V_t}\right)-1\right]\frac{1}{\sqrt{E_{hlis}+1}} \\ Q_{bddif} &= tW_{eff}{}'T_{si}J_{sbjt}\left[1+L_{dif0}\left(L_{bjt0}\left(\frac{1}{L_{eff}}+\frac{1}{L_n}\right)^{N_{dif}}\right)\right]\left[\exp\left(\frac{V_{bd}}{n_{dio}V_t}\right)-1\right]\frac{1}{\sqrt{E_{hlid}+1}} \end{aligned} \tag{4.15}$$

The parameter t represents the transit time of the injected minority carriers in the body. The parameters L_{dif0} and N_{dif} are provided to better fit the data.

4.4. Extrinsic Capacitances

Expressions for extrinsic (parasitic) capacitances that are common in bulk and SOI MOSFETs are taken directly from BSIM3v3. They are source/drain-to-gate overlap capacitance and source/drain-to-gate fringing capacitance. Additional SOI-specific parasitics added are substrate-to-source sidewall capacitance C_{essw}, and substrate-to-drain sidewall capacitance C_{edsw}, substrate-to-source bottom capacitance (C_{esb}) and substrate-to-drain bottom capacitance (C_{edb}) [Fig. 4.2].

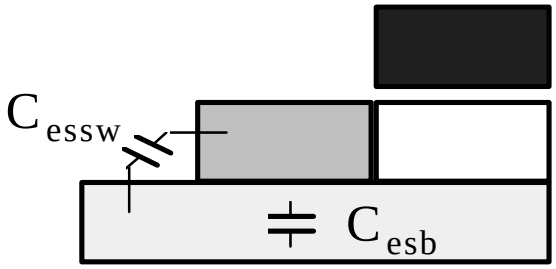


Fig. 4.2 SOI MOSFET extrinsic charge components. C_{essw} is the substrate-to-source sidewall capacitance. C_{esb} is the substrate-to-source bottom capacitance.

In SOI, there is a parasitic source/drain-buried oxide-Si substrate parasitic MOS structure with a bias dependent capacitance. If $V_{s,d}$=0, this MOS structure might be in accumulation. However, if $V_{s,d}=V_{dd}$, the MOS structure is in depletion with a much smaller capacitance, because the Si substrate is lightly doped. The bias dependence of this capacitance is similar to high frequency MOS depletion capacitance as shown in Fig. 4.3. It might be substantial in devices with large source/drain diffusion areas. BSIMPD models it by piece-wise expressions, with accurately chosen parameters to achieve smoothness of capacitance and continuity to the second derivative of charge. The substrate-to-source bottom capacitance (per unit source/drain area) C_{esb} is:

$$C_{esb}=\begin{cases} C_{box} & if \quad V_{se}<V_{sdfb} \\ C_{box}-\dfrac{1}{A_{sd}}\left(C_{box}-C_{\min}\right)\left(\dfrac{V_{se}-V_{sdfb}}{V_{sdth}-V_{sdfb}}\right)^2 & elseif \quad V_{se}<V_{sdfb}+A_{sd}\left(V_{sdth}-V_{sdfb}\right) \\ C_{\min}+\dfrac{1}{1-A_{sd}}\left(C_{box}-C_{\min}\right)\left(\dfrac{V_{se}-V_{sdth}}{V_{sdth}-V_{sdfb}}\right)^2 & elseif \quad V_{se}<V_{sdth} \\ C_{\min} & else \end{cases} \tag{4.16}$$

Physical parameters V_{sdfb} (flat-band voltage of the MOS structure) and V_{sdth} (threshold voltage of the MOS structure) can be easily extracted from measurement. C_{min} should also be extracted from measurement, and it can account for deep depletion as well. A_{sd} is a smoothing parameter.

The expression for C_{edb} is similar to C_{esb}. Fig. 4.3 shows the comparison of the model and measured C_{esb}.

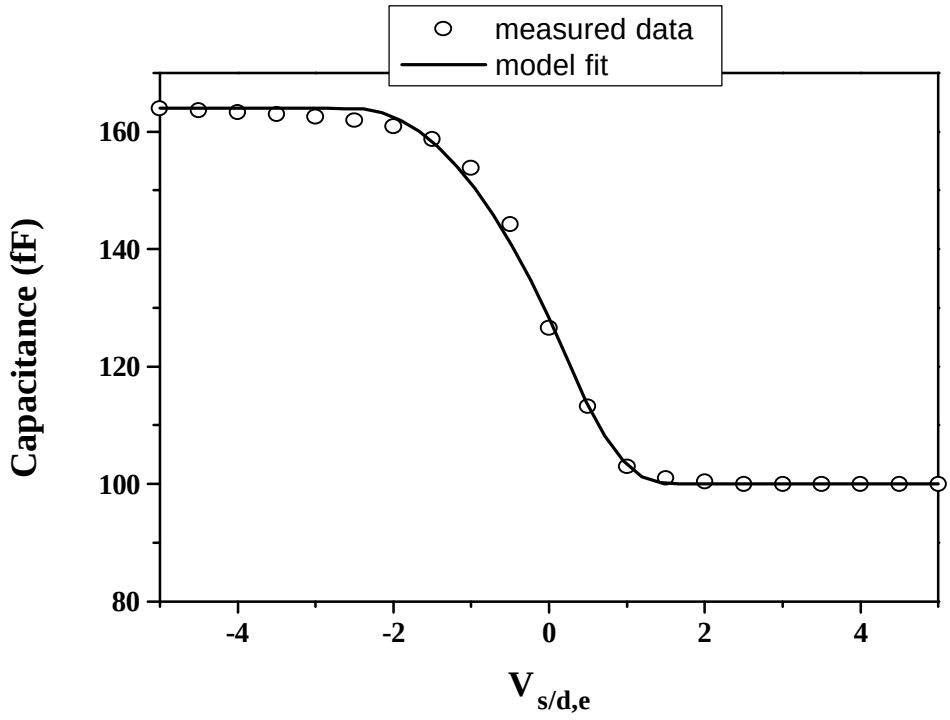


Fig. 4.3 Bottom source/drain to substrate capacitance for a PD SOI MOSFET.

Finally, the sidewall source/drain to substrate capacitance (per unit source/drain perimeter length) can be expressed by

$$C_{s/d,esw} = C_{sdesw} \log\left(1 + \frac{T_{si}}{T_{box}}\right) \tag{4.17}$$

which depends on the silicon film thickness T_{si} and the buried oxide thickness T_{box}. The parameter C_{sdesw} represents the fringing capacitance per unit length.

4.5. Body Contact Parasitics

The parasitic capacitive coupling due to the body contact is considered in BSIMPD. The

instance parameter A_{gbcp} represents the parasitic gate-to-body overlap area due to the body contact, and A_{ebcp} represents the parasitic substrate-to-body overlap area. The effect may be significant for small area devices [CV part in Appendix C].

Chapter 5: Temperature Dependence and Self-Heating

Self-heating in SOI is more important than in bulk since the thermal conductivity of silicon dioxide is about two orders of magnitude lower than that of silicon [15]. It may degrade the carrier mobility, increase the junction leakage [20], enhance the impact ionization rate[24], and therefore affect the output characteristics [16] of floating-body SOI devices.

5.1. Temperature Dependence

The temperature dependence of threshold voltage, mobility, saturation velocity and series resistance in BSIMPD is identical to BSIM3v3. However a different temperature dependence of diode characteristics is adopted in BSIMPD:

$$j_{sbjt} = j_{sbjt0}\exp\left[\frac{-E_g(300K)}{n_{dio}V_t}X_{bjt}\left(1-\frac{T}{T_{nom}}\right)\right]$$

$$j_{sdif} = j_{sdif0}\exp\left[\frac{-E_g(300K)}{n_{dio}V_t}X_{dif}\left(1-\frac{T}{T_{nom}}\right)\right]$$

$$j_{srec} = j_{srec0}\exp\left[\frac{-E_g(300K)}{n_{recf0}V_t}X_{rec}\left(1-\frac{T}{T_{nom}}\right)\right]$$

$$j_{stun} = j_{stun0}\exp\left[X_{tun}\left(\frac{T}{T_{nom}}-1\right)\right] \tag{5.1}$$

$$\boldsymbol{n_{recf} = n_{recf0}\left[1+nt_{recf}\left(\frac{T}{T_{nom}}-1\right)\right]}$$

$$\boldsymbol{n_{recr} = n_{recr0}\left[1+nt_{recr}\left(\frac{T}{T_{nom}}-1\right)\right]}$$

The parameters $j_{sbjt0}, j_{sdif0}, j_{srec0}, j_{stun0}$ are diode saturation currents at the nominal temperature T_{nom}, and the parameters $X_{bjt}, X_{dif}, X_{rec}, X_{tun}$ are provided to model the temperature dependence.

Notice that the non-ideality factors n_{recf}, n_{recr} are also temperature dependent.

5.2. Self-Heating Implementation

BSIMPD models the self-heating by an auxiliary $R_{th}C_{th}$ circuit as shown in Fig. 5.1 [18]. The temperature node (T node) will be created in SPICE simulation if the self-heating selector *shMod* is ON and the thermal resistance is non-zero. The T node is treated as a voltage node and is connected to ground through a thermal resistance R_{th} and a thermal capacitance C_{th}:

$$R_{th} = \frac{R_{th0}}{W'_{eff} + W_{th0}}, \; C_{th} = C_{th0}(W'_{eff} + W_{th0}) \tag{5.2}$$

where R_{th0} and C_{th0} are normalized thermal resistance and capacitance, respectively. W_{th0} is the minimum width for thermal resistance calculation [19]. Notice that the current source is driving a current equal to the power dissipated in the device.

$$P = \left| I_{ds} \times V_{ds} \right| \tag{5.3}$$

To save computation time, the turn-on surface potential ϕ_s (Phi) is taken to be a constant within each timepoint because a lot of parameters (e.g. X_{dep}) are function of ϕ_s. Each timepoint will use a ϕ_s calculated with the temperature iterated in the previous timepoint. However this approximation may induce error in DC, transient and AC simulation. Therefore, it is a tradeoff between accuracy and speed. The error in DC or transient is minimal if the sweeping step or time step is sufficiently small.

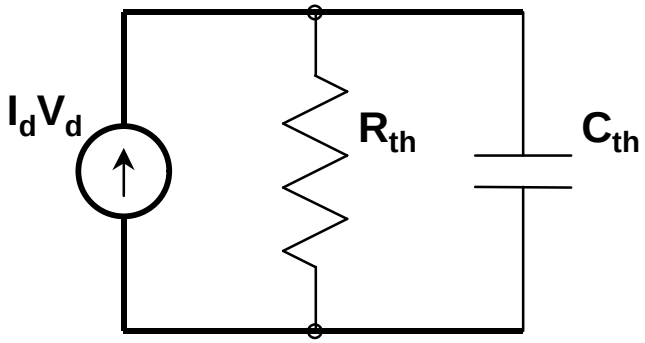


Fig. 5.1 Equivalent circuit for self-heating simulation.

Chapter 6: BSIMSOI –

A Unified Model for PD and FD SOI MOSFETs

Using BSIMPD as a foundation, we have developed a unified model for both PD and FD SOI circuit designs based on the concept of *body-source built-in potential lowering* [20, 25].

6.1. BSIMSOI Framework and Built-In Potential Lowering Model

As described in [20], we construct BSIMSOI based on the concept of body-source built-in potential lowering, ΔV_{bi}. There are three modes (soiMod = 0, 1, 2) in BSIMSOI: BSIMPD (soiMod = 0) can be used to model the PD SOI device, where the body potential is independent on ΔV_{bi} ($V_{BS} > \Delta V_{bi}$). Therefore the calculation of ΔV_{bi} is skipped in this mode. On the other hand, the ideal FD model (soiMod = 2) is for the FD device with body potential equal to ΔV_{bi}. Hence the calculation of body current/charge, which is essential to the PD model, is skipped. For the unified SOI model (soiMod = 1), however, both ΔV_{bi} and body current/charge are calculated to capture the floating-body behavior exhibited in FD devices. As shown in Figure 6.1, this unified model covers both BSIMPD and the ideal FD model.

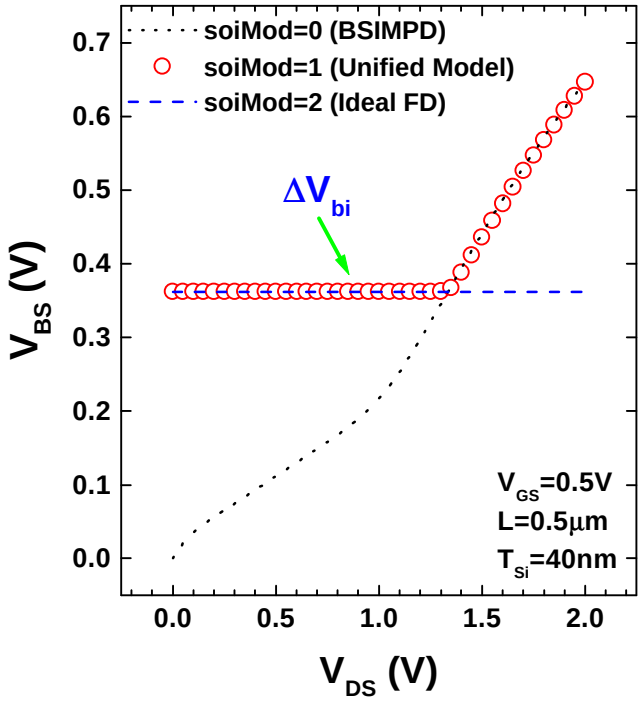


Fig. 6.1 The body potential in the unified model approaches the V_{BS} solved in BSIMPD for PD devices, while returns to ΔV_{bi} for ideal FD devices [20].

This unified model shares the same floating-body module as BSIMPD, with a generalized diode current model considering the body-source built-in potential lowering effect ($I_{BS} \propto \exp(-q\Delta V_{bi}/kT)$). Therefore, an accurate and efficient ΔV_{bi} model is crucial. The following formulation for ΔV_{bi} is mainly based on the Poisson equation and the physical characterization for ΔV_{bi}, as presented in [25].

For a given surface band bending ϕ (source reference), ΔV_{bi} can be formulated by applying the Poisson equation in the vertical direction and continuity of normal displacement at the back interface:

$$\Delta V_{bi}(f) = \frac{C_{Si}}{C_{Si}+C_{BOX}} \cdot \left(f - \frac{qN_{ch}}{2e_{Si}} \cdot T_{Si}^{\,2} + \Delta V_{DIBL} \right) + h_e(L_{eff}) \frac{C_{BOX}}{C_{Si}+C_{BOX}} \cdot (V_{bGS} - V_{FBb})$$
$$C_{Si} = \frac{e_{Si}}{T_{Si}}, C_{BOX} = \frac{e_{OX}}{T_{BOX}}, C_{OX} = \frac{e_{OX}}{T_{OX}} \qquad (6\text{-}1).$$

The first term of Equation (6-1) represents the frontgate coupling. T_{Si} is the SOI thickness. N_{ch} accounts for the effective channel doping, which may vary with channel length due to the non-uniform lateral doping effect. The second term of Equation (6-1) represents the backgate coupling (V_{bGS}). V_{FBb} is the backgate flatband voltage. Equation (6-1) shows that the impact of frontgate on ΔV_{bi} reaches maximum when the buried oxide thickness, $T_{BOX,}$ approaches infinity.

In Equation (6-1), ΔV_{DIBL} represents the short channel effect on ΔV_{bi},

$$\Delta V_{DIBL} = D_{vbd0}\left(exp\left(-D_{vbd1}\frac{L_{eff}}{2l} \right) + 2exp\left(-D_{vbd1}\frac{L_{eff}}{l} \right) \right) \cdot (V_{bi} - 2\Phi_B) \qquad (6\text{-}2),$$

as addressed in [25]. Here *l* is the characteristic length for the short-channel-effect calculation. D_{vbd0} and D_{vbd1} are model parameters. Similarly, the following equation

$$h_e(L_{eff}) = K_{1b} - K_{2b} \cdot \left(exp\left(-D_{k2b}\frac{L_{eff}}{2l} \right) + 2exp\left(-D_{k2b}\frac{L_{eff}}{l} \right) \right) \qquad (6\text{-}3)$$

is used to account for the short channel effect on the backgate coupling, as described in [25]. D_{K1b}, D_{K2b}, K_{1b} (default 1) and K_{2b} (default 0) are model parameters.

The surface band bending, ϕ, is determined by the frontgate V_{GS} and may be approximated by

$$f = \begin{cases} \Phi_{ON} & \text{for } V_{GS} \geq V_T \\ \Phi_{ON} - \dfrac{C_{OX}}{C_{OX} + \left(C_{Si}^{-1} + C_{BOX}^{-1}\right)^{-1}} \cdot \left(V_T - V_{GS}\right) & \text{for } V_{GS} \leq V_T \end{cases} \quad \text{(6-4).}$$

To improve the simulation convergency, the following single continuous function from subthreshold to strong inversion is used:

$$f = \Phi_{ON} - \frac{C_{OX}}{C_{OX} + \left(C_{Si}^{-1} + C_{BOX}^{-1}\right)^{-1}} \cdot N_{OFF,FD} V_t \cdot ln\left(1 + exp\left(\frac{V_{T,FD} - V_{gs\_eff} - V_{OFF,FD}}{N_{OFF,FD} V_t}\right)\right) \quad \text{(6-5).}$$

Here V_{gs_eff} is the effective gate bias considering the poly-depletion effect. $V_{T,FD}$ is the threshold voltage at $V_{BS} = \Delta V_{bi}(\phi=2\Phi_B)$. $N_{OFF,FD}$ (default 1) and $V_{OFF,FD}$ (default 0) are model parameters introduced to improve the transition between subthreshold and strong inversion. V_t is the thermal voltage. Notice that the frontgate coupling ratio in the subthreshold regime approaches 1 as T_{BOX} approaches infinity.

To accurately model ΔV_{bi} and thus the device output characteristics, the surface band bending at strong inversion, Φ_{ON}, is not pinned at $2\Phi_B$. Instead, the following equation

$$\Phi_{ON} = 2\Phi_B + V_t\, ln\left(1 + \frac{V_{gsteff.FD}\left(V_{gsteff,FD} + 2K1\sqrt{2\Phi_B}\right)}{moin \cdot K1 \cdot V_t^{\,2}}\right) \quad \text{(6-6)}$$

is used to account for the surface potential increment with gate bias in the strong inversion regime [4]. Here *moin* is a model parameter. K1 is the body effect coefficient. Notice that a single continuous function,

$$V_{gsteff,FD} = N_{OFF,FD} V_t \cdot ln\left(1 + exp\left(\frac{V_{gs\_eff} - V_{T,FD} - V_{OFF,FD}}{N_{OFF,FD} V_t}\right)\right) \quad \text{(6-7),}$$

has been used to represent the gate overdrive in Equation (6-6).

6.2. Verification

The BSIMPD parameter extraction methodology presented in [20] may still be used under the unified BSIMSOI framework, provided that the link between PD and FD, ΔV_{bi}, can be accurately extracted. As described in [25], a direct probe of ΔV_{bi} can be achieved by finding the onset of the external body bias (through a body contact) after which the threshold voltage and hence the channel current of the FD SOI device is modulated. When the body contact is not available, nevertheless, model parameters related to ΔV_{bi} should be extracted based on the subthreshold characteristics of the floating-body device. As shown in Figure 6.2, the reduction of ΔV_{bi} with backgate bias is responsible for the transition from the ideal subthreshold swing (~ 60 mV/dec. at room temperature) to the non-ideal one.

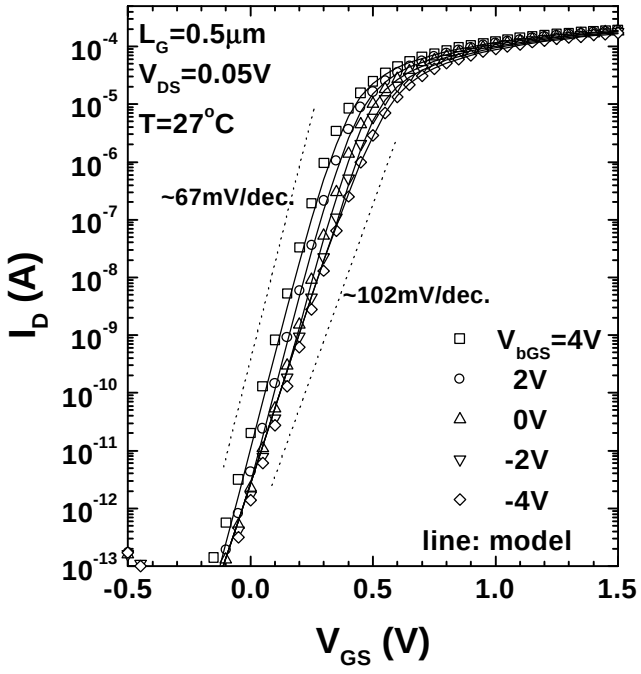


Fig. 6.2 The PD/FD transition can be captured by modeling ΔV_{bi} [20].

Figure 6.2 clearly shows that the PD/FD transition can be captured by the ΔV_{bi} approach. In other words, ΔV_{bi} is indeed an index of the degree of full depletion, as pointed out in [20, 25]. As shown in Figure 6.3, larger floating-body effect can be observed for negative backgate bias due to smaller ΔV_{bi}. In case the ΔV_{bi} value is raised by charge sharing as described in [25], it can be predicted that the short-channel device should exhibit less floating-body effect than the long-channel one due to larger ΔV_{bi}, as verified in Figure 6.4.

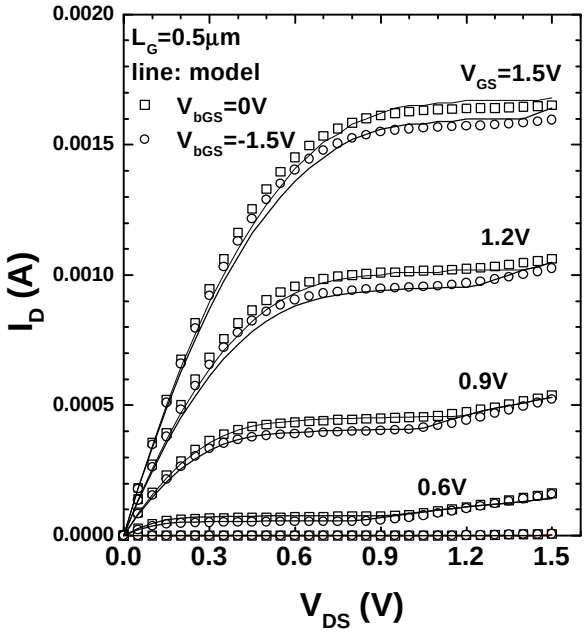


Fig. 6.3 Larger floating-body effect can be seen for the negative backgate bias (source reference) due to smaller ΔV_{bi} [20].

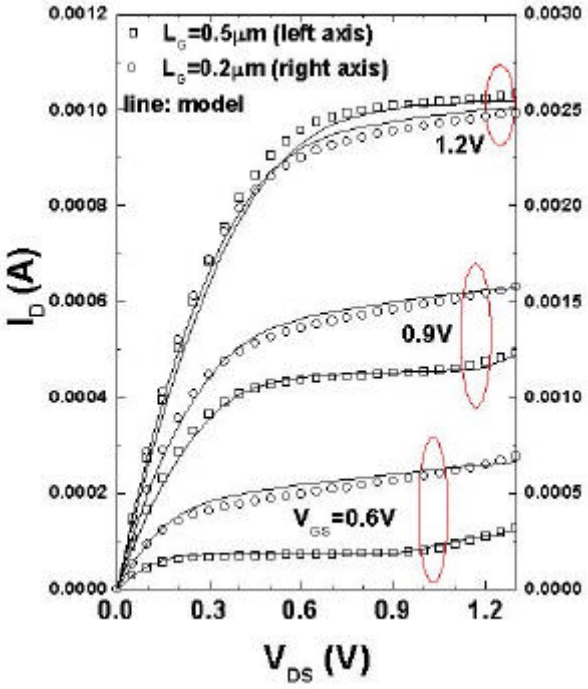


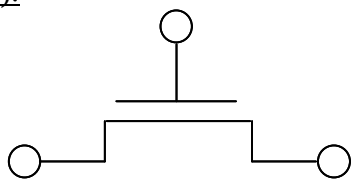
Fig. 6.4 Less floating-body effect can be seen for the short-channel device due to larger ΔV_{bi} [20].

Chapter 7: BSIMSOI RF model

RF Model in BSIMSOIv3.1

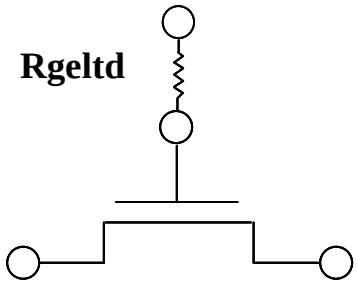
BSIMSOI3.1 provides the gate resistance model for devices used in RF application. Users have four options for modeling gate electrode resistance (bias independent) and intrinsic-input resistance (Rii, bias-dependent) by choosing model choice parameter rgateMod.

RgateMod = 0 (zero-resistance):



In this case, no gate resistance is generated.

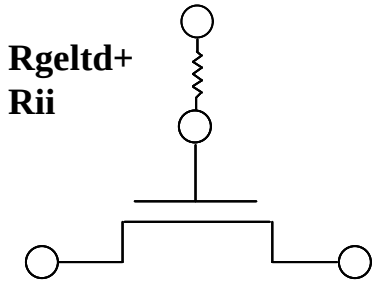
RgateMod = 1 (constant-resistance):



In this case, only the electrode gate resistance (bias-independent) is generated by adding an internal gate node. The electrode gate resistance Rgeltd is given by

$$Rgeltd = \frac{RSHG \cdot \left(XGW + \frac{W_{eff}}{3 \cdot NGCON \cdot NSEG} \right)}{NGCON \cdot \left(L_{drawn} - XGL \right)}$$

RgateMod = 2 (RII model with variable resistance):



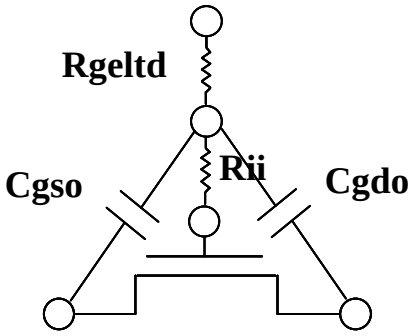
In this case, the gate resistance is the sum of the electrode gate resistance and the intrinsic-input resistance Rii as given by

$$\frac{1}{Rii} = XRCRG1 \cdot \left(\frac{I_{ds}}{V_{dseff}} + XRCRG2 \cdot \frac{W_{eff} m_{eff} C_{oxeff} k_B T}{q L_{eff}} \right)$$

An internal gate node will be generated.

RgateMod = 3 (RII model with two nodes):

In this case, the gate electrode resistance is in series with the intrinsic-input resistance Rii through two internal gate nodes, so that the overlap capacitance current will not pass through the intrinsic-input resistance.



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Appendix A: Model Instance Syntax

```
Mname <D node> <G node> <S node> <E node> [P node]
      [B node] [T node] <model>
      [L=<val>] [W=<val>]
      [AD=<val>] [AS=<val>] [PD=<val>] [PS=<val>]
      [NRS=<val>] [NRD=<val>] [NRB=<val>]
      [OFF][BJTOFF=<val>]
      [IC=<val>,<val>,<val>,<val>,<val>]
      [RTH0=<val>] [CTH0=<val>]
      [DEBUG=<val>]
      [NBC=<val>] [NSEG=<val>] [PDBCP=<val>] [PSBCP=<val>]
      [AGBCP=<val>][AEBCP=<val>][VBSUSR=<val>][TNODEOUT]
      [FRBODY=<val>]
```

A.1. Description

<D node>	Drain node
<G node>	Gate node
<S node>	Source node
<E node>	Substrate node
[P node]	(Optional) external body contact node
[B node]	(Optional) internal body node
[T node]	(Optional) temperature node
<model>	Level 9 BSIM3SOI model name
[L]	Channel length
[W]	Channel width
[AD]	Drain diffusion area
[AS]	Source diffusion area
[PD]	Drain diffusion perimeter length

[PS]	Source diffusion perimeter length
[NRS]	Number of squares in source series resistance
[NRD]	Number of squares in drain series resistance
[NRB]	Number of squares in body series resistance
[OFF]	Device simulation off
[BJTOFF]	Turn off BJT current if equal to 1
[IC]	Initial guess in the order of (Vds, Vgs, Vbs, Ves, Vps). (Vps will be ignored in the case of 4-terminal device)
[RTH0]	Thermal resistance per unit width ■ if not specified, RTH0 is extracted from model card. ■ if specified, it will override the one in model card.
[CTH0]	Thermal capacitance per unit width ■ if not specified, CTH0 is extracted from model card. ■ if specified, it will over-ride the one in model card.
[DEBUG]	Please see the debugging notes
[NBC]	**Number of body contact isolation edge**
[NSEG]	**Number of segments for channel width partitioning [17]**
[PDBCP]	**Parasitic perimeter length for body contact at drain side**
[PSBCP]	**Parasitic perimeter length for body contact at source side**
[AGBCP]	**Parasitic gate-to-body overlap area for body contact**
[AEBCP]	**Parasitic body-to-substate overlap area for body contact**
[VBSUSR]	**Optional initial value of Vbs specified by user for transient analysis**
[TNODEOUT]	**Temperature node flag indicating the usage of T node**
[FRBODY]	**Layout-dependent body resistance coefficient**

A.2. About Optional Nodes

There are three optional nodes, P, B and T nodes. P and B nodes are used for body contact devices. Let us consider the case when TNODEOUT is not set. If user specifies four nodes, this element is a 4-terminal device, i.e., floating body. If user specifies five nodes, the fifth node represents the external body contact node (P). There is a body resistance between internal body node and P node. In these two cases, an internal body node is created but it is not accessible in the circuit deck. If user specifies six nodes, the fifth node represents the P node and the sixth node represents the internal body node (B). This configuration is useful for distributed body resistance simulation.

If TNODEOUT flag is set, the last node is interpreted as the temperature node. In this case, if user specifies five nodes, it is a floating body case. If user specifies six nodes, it is a body-contacted case. Finally, if user specifies seven nodes, it is a body-contacted case with an accessible internal body node. The temperature node is useful for thermal coupling simulation.

A.3. Notes on Debugging

The instance parameter <DEBUG> allows users to turn on debugging information selectively. Internal parameters (e.g. par) for an instance (e.g. m1) can be plotted by this command:

plot m1#par

By default, <DEBUG> is set to zero and two internal parameters will be available for plotting:

#body	V_b value iterated by SPICE
#temp	Device temperature with self-heating mode turned on

If <DEBUG> is set to one or minus one, more internal parameters are available for plotting. This serves debugging purposes when there is a convergence problem. This can also help the user to understand the model more. For <DEBUG> set to minus one, there will be charge calculation even if the user is running DC simulation. Here is the list of internal parameters:

#Vbs	Real V_{bs} value used by the IV calculation
#Vgsteff	Effective gate-overdrive voltage
#Vth	Threshold voltage
#Ids	MOS drain current
#Ic	BJT current
#Ibs	Body to source diode current
#Ibd	Body to drain diode current
#Iii	Impact ionization current
#Igidl	GIDL current
#Itun	Tunneling current
#Ibp	Body contact current
#Gds	Output conductance
#Gm	Transconductance
#Gmb	Drain current derivative wrt Vbs

These parameters are valid only if charge computation is required

#Cbb	Body charge derivative wrt Vbs
#Cbd	Body charge derivative wrt Vds
#Cbe	Body charge derivative wrt Ves
#Cbg	Body charge derivative wrt Vgs
#Qbody	Total body charge
#Qgate	Gate charge
#Qac0	Accumulation charge
#Qsub	Bulk charge
#Qsub0	Bulk charge at zero drain bias
#Qbf	Channel depletion charge
#Qjd	Parasitic drain junction charge
#Qjs	Parasitic source junction charge

Appendix B: Model Parameter List

All model parameters additional to BSIM3v3 will be shown with bold cases.

B.0. BSIMSOI Built-In Potential Lowering (ΔV_{bi}) Model Parameters

Symbol used in equation	Symbol used in SPICE	Description	Unit	Default
SoiMod	soiMod	SOI model selector. SoiMod=0: BSIMPD. SoiMod=1: unified model for PD&FD. SoiMod=2: ideal FD.	-	0
$V_{nonideal}$	vbsa	Offset voltage due to non-idealities	V	0
$N_{OFF,FD}$	nofffd	Smoothing parameter in FD module	-	1
$V_{OFF,FD}$	vofffd	Smoothing parameter in FD module	V	0
K_{1b}	K1b	First backgate body effect parameter	-	1
K_{2b}	K2b	Second backgate body effect parameter for short channel effect	-	0
D_{k2b}	dk2b	Third backgate body effect parameter for short channel effect	-	0
D_{vbd0}	dvbd0	First short channel effect parameter in FD module	-	0
D_{vbd1}	dvbd1	Second short channel effect parameter in FD module	-	0
MoinFD	moinfd	Gate bias dependence coefficient of surface potential in FD module	-	1e3

B.1. BSIMPD Model Control Parameters

Symbol used in equation	Symbol used in SPICE	Description	Unit	Default	Notes (below the table)
None	**level**	**Level 9 for BSIM3SOI**	**-**	**9**	**-**
Shmod	**shMod**	**Flag for self-heating** **0 - no self-heating,** **1 - self-heating**	**-**	**0**	
Mobmod	mobmod	Mobility model selector	-	1	-
Capmod	capmod	Flag for the short channel capacitance model	-	2	**nI-1**
Noimod	noimod	Flag for Noise model	-	1	-
RgateMod	rgateMod	Gate resistance model selector	-	0	-

B.2. Process Parameters

Symbol used in equation	Symbol used in SPICE	Description	Unit	Default	Notes (below the table)
t_{si}	**Tsi**	**Silicon film thickness**	**m**	**10^{-7}**	-
t_{box}	**Tbox**	**Buried oxide thickness**	**m**	**$3x10^{-7}$**	-
t_{ox}	Tox	Gate oxide thickness	m	$1x10^{-8}$	-
X_j	Xj	S/D junction depth	m	**nI-2**	-
n_{ch}	Nch	Channel doping concentration	$1/cm^3$	$1.7x10^{17}$	-
n_{sub}	Nsub	Substrate doping concentration	$1/cm^3$	$6x10^{16}$	**nI-3**
Ngate	ngate	poly gate doping concentration	$1/cm^3$	0	-

B.3. DC Parameters

Symbol used in equation	Symbol used in SPICE	Description	Unit	Default	Notes (below the table)
V_{th0}	vth0	Threshold voltage @V_{bs}=0 for long and wide device	-	0.7	-
K_1	k1	First order body effect coefficient	$V^{1/2}$	0.6	-
K_{1w1}	**k1w1**	**First body effect width dependent parameter**	**m**	**0**	-
K_{1w2}	**k1w2**	**Second body effect width dependent parameter**	**m**	**0**	-
K_2	k2	Second order body effect coefficient	-	0	-
K_3	k3	Narrow width coefficient	-	0	-
K_{3b}	k3b	Body effect coefficient of k3	1/V	0	-
K_{b1}	Kb1	Backgate body charge coefficient	-	1	-

W_0	w0	Narrow width parameter	m	0	-
N_{LX}	nlx	Lateral non-uniform doping parameter	m	1.74e-7	-
D_{vt0}	Dvt0	first coefficient of short-channel effect on Vth	-	2.2	-
D_{vt1}	dvt1	Second coefficient of short-channel effect on Vth	-	0.53	-
D_{vt2}	dvt2	Body-bias coefficient of short-channel effect on Vth	1/V	-0.032	-
D_{vt0w}	dvt0w	first coefficient of narrow width effect on Vth for small channel length	-	0	-
D_{vt1w}	dvt1w	Second coefficient of narrow width effect on Vth for small channel length	-	5.3e6	-
D_{vt2w}	dvt2w	Body-bias coefficient of narrow width effect on Vth for small channel length	1/V	-0.032	-
m_0	u0	Mobility at Temp = Tnom NMOSFET PMOSFET	$cm^2/(V\text{-}sec)$	 670 250	-
U_a	ua	First-order mobility degradation coefficient	m/V	2.25e-9	-
U_b	ub	Second-order mobility degradation coefficient	$(m/V)^2$	5.9e-19	-
U_c	uc	Body-effect of mobility degradation coefficient	1/V	-.0465	-
v_{sat}	vsat	Saturation velocity at Temp=Tnom	m/sec	8e4	-
$A0$	a0	Bulk charge effect coefficient for channel length	-	1.0	-
A_{gs}	ags	Gate bias coefficient of A_{bulk}	1/V	0.0	-
$B0$	b0	Bulk charge effect coefficient for channel width	m	0.0	-

B1	b1	Bulk charge effect width offset	m	0.0	-
Keta	keta	Body-bias coefficient of bulk charge effect	V^{-1}	0	-
Ketas	**Ketas**	**Surface potential adjustment for bulk charge effect**	**V**	**0**	-
A_1	A1	First non-saturation effect parameter	1/V	0.0	-
A_2	A2	Second non-saturation effect parameter	0	1.0	-
R_{dsw}	rdsw	Parasitic resistance per unit width	Ω-μm^{Wr}	100	-
Prwb	prwb	Body effect coefficient of Rdsw	1/V	0	-
Prwg	prwg	Gate bias effect coefficient of Rdsw	$1/V^{1/2}$	0	-
Wr	wr	Width offset from Weff for Rds calculation	-	1	-
Nfactor	nfactor	Subthreshold swing factor	-	1	-
Wint	wint	Width offset fitting parameter from I-V without bias	m	0.0	-
Lint	lint	Length offset fitting parameter from I-V without bias	m	0.0	-
DWg	dwg	Coefficient of W_{eff}'s gate dependence	m/V	0.0	
DWb	dwb	Coefficient of W_{eff}'s substrate body bias dependence	$m/V^{1/2}$	0.0	
DWbc	**Dwbc**	**Width offset for body contact isolation edge**	**m**	**0.0**	
V_{off}	voff	Offset voltage in the subthreshold region for large W and L	V	-0.08	-
Eta0	eta0	DIBL coefficient in subthreshold region	-	0.08	-
Etab	etab	Body-bias coefficient for the subthreshold DIBL effect	1/V	-0.07	-
D_{sub}	dsub	DIBL coefficient exponent	-	0.56	-

C_{it}	cit	Interface trap capacitance	F/m^2	0.0	-
C_{dsc}	cdsc	Drain/Source to channel coupling capacitance	F/m^2	2.4e-4	-
C_{dscb}	cdscb	Body-bias sensitivty of C_{dsc}	F/m^2	0	-
C_{dscd}	cdscd	Drain-bias sensitivty of C_{dsc}	F/m^2	0	-
P_{clm}	pclm	Channel length modulation parameter	-	1.3	-
P_{dibl1}	pdibl1	First output resistance DIBL effect correction parameter	-	.39	-
P_{dibl2}	pdibl2	Second output resistance DIBL effect correction parameter	-	0.086	-
D_{rout}	drout	L dependence coefficient of the DIBL correction parameter in Rout	-	0.56	-
Pvag	pvag	Gate dependence of Early voltage	-	0.0	-
d	delta	Effective V_{ds} parameter	-	0.01	-
a_0	alpha0	The first parameter of impact ionization current	m/V	0.0	-
F_{bjtii}	**fbjtii**	**Fraction of bipolar current affecting the impact ionization**	-	**0.0**	-
b_0	**beta0**	**First V_{ds} dependent parameter of impact ionization current**	**V^{-1}**	**0**	-
b_1	**beta1**	**Second V_{ds} dependent parameter of impact ionization current**	-	**0**	-
b_2	**beta2**	**Third V_{ds} dependent parameter of impact ionization current**	**V**	**0.1**	-
$V_{dsatii0}$	**vdsatii0**	**Nominal drain saturation voltage at threshold for impact ionization current**	**V**	**0.9**	-
T_{ii}	**tii**	**Temperature dependent parameter for impact ionization current**	-	**0**	-

L_{ii}	lii	Channel length dependent parameter at threshold for impact ionization current	-	0	-
E_{satii}	esatii	Saturation channel electric field for impact ionization current	V/m	1e7	-
S_{ii0}	sii0	First V_{gs} dependent parameter for impact ionization current	V^{-1}	0.5	-
S_{ii1}	sii1	Second V_{gs} dependent parameter for impact ionization current	V^{-1}	0.1	-
S_{ii2}	sii2	Third V_{gs} dependent parameter for impact ionization current	-	0	-
S_{iid}	siid	V_{ds} dependent parameter of drain saturation voltage for impact ionization current	V^{-1}	0	-
a_{gidl}	Agidl	GIDL constant	Ω^{-1}	0.0	-
b_{gidl}	Bgidl	GIDL exponential coefficient	V/m	0.0	-
c	Ngidl	GIDL V_{ds} enhancement coefficient	V	1.2	-
n_{tun}	Ntun	Reverse tunneling non-ideality factor	-	10.0	-
n_{diode}	Ndio	Diode non-ideality factor	-	1.0	-
n_{recf0}	Nrecf0	Recombination non-ideality factor at forward bias	-	2.0	-
n_{recr0}	Nrecr0	Recombination non-ideality factor at reversed bias	-	10	-
i_{sbjt}	Isbjt	BJT injection saturation current	A/m^2	1e-6	-
i_{sdif}	Isdif	Body to source/drain injection saturation current	A/m^2	1e-7	-
i_{srec}	Isrec	Recombination in depletion saturation current	A/m^2	1e-5	-
i_{stun}	Istun	Reverse tunneling saturation current	A/m^2	0.0	-

Ln	**Ln**	**Electron/hole diffusion length**	**m**	**2e-6**	**-**
V_{rec0}	**Vrec0**	**Voltage dependent parameter for recombination current**	**V**	**0**	**-**
V_{tun0}	**Vtun0**	**Voltage dependent parameter for tunneling current**	**V**	**0**	**-**
N_{bjt}	**Nbjt**	**Power coefficient of channel length dependency for bipolar current**	**-**	**1**	**-**
L_{bjt0}	**Lbjt0**	**Reference channel length for bipolar current**	**m**	**0.20e-6**	**-**
V_{abjt}	**Vabjt**	**Early voltage for bipolar current**	**V**	**10**	**-**
A_{ely}	**Aely**	**Channel length dependency of early voltage for bipolar current**	**V/m**	**0**	**-**
A_{hli}	**Ahli**	**High level injection parameter for bipolar current**	**-**	**0**	**-**
Rbody	**Rbody**	**Intrinsic body contact sheet resistance**	**ohm/square**	**0.0**	**-**
Rbsh	**Rbsh**	**Extrinsic body contact sheet resistance**	**ohm/square**	**0.0**	**-**
Rsh	rsh	Source drain sheet resistance in ohm per square	ohm/square	0.0	-
Rhalo	rhalo	Body halo sheet resistance	**ohm/m**	**1e15**	-

B.4. Gate-to-body tunneling parameters

Symbol used in equation	Symbol used in SPICE	Description	Unit	Default
IgMod	igMod	Gate current model selector	-	0
Toxqm	toxqm	Oxide thickness for I_{gb} calculation	m	Tox
Ntox	ntox	Power term of gate current	-	1
Toxref	toxref	Target oxide thickness	m	2.5e-9
j_g	ebg	Effective bandgap in gate current calculation	V	1.2
a_{gb1}	alphaGB1	First Vox dependent parameter for gate current in inversion	1/V	.35
b_{gb1}	betaGB1	Second Vox dependent parameter for gate current in inversion	$1/V^2$	.03
V_{gb1}	vgb1	Third Vox dependent parameter for gate current in inversion	V	300
V_{EVB}	vevb	Vaux parameter for valence band electron tunneling	-	0.075
a_{gb2}	alphaGB2	First Vox dependent parameter for gate current in accumulation	1/V	.43
b_{gb2}	betaGB2	Second Vox dependent parameter for gate current in accumulation	$1/V^2$	.05
V_{gb2}	vgb2	ThirdVox dependent parameter for gate current in accumulation	V	17
V_{ECB}	vecb	Vaux parameter for conduction band electron tunneling	-	.026

B.5. AC and Capacitance Parameters

Symbol used in equation	Symbol used in SPICE	Description	Unit	Default	Notes (below the table)
Xpart	xpart	Charge partitioning rate flag	-	0	
CGS0	cgso	Non LDD region source-gate overlap capacitance per channel length	F/m	calcu-lated	**nC-1**
CGD0	cgdo	Non LDD region drain-gate overlap capacitance per channel length	F/m	calcu-lated	**nC-2**
CGEO	**cgeo**	**Gate substrate overlap capacitance per unit channel length**	**F/m**	**0.0**	**-**
Cjswg	cjswg	Source/Drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm T_{si})	F/m^2	1e-10	-
Pbswg	pbswg	Source/Drain (gate side) sidewall junction capacitance buit in potential	V	.7	-
Mjswg	mjswg	Source/Drain (gate side) sidewall junction capacitance grading coefficient	V	0.5	-
t_t	**tt**	**Diffusion capacitance transit time coefficient**	**second**	**1e-12**	**-**
N_{dif}	**Ndif**	**Power coefficient of channel length dependency for diffusion capacitance**	**-**	**-1**	**-**
L_{dif0}	**Ldif0**	**Channel-length dependency coefficient of diffusion cap.**	**-**	**1**	**-**
V_{sdfb}	**vsdfb**	**Source/drain bottom diffusion capacitance flatband voltage**	**V**	**calcu-lated**	**nC-3**
V_{sdth}	**vsdth**	**Source/drain bottom diffusion**	**V**	**calcu-**	**nC-4**

		capacitance threshold voltage		**lated**	
C_{sdmin}	**csdmin**	**Source/drain bottom diffusion minimum capacitance**	**V**	**calcu-lated**	**nC-5**
A_{sd}	**asd**	**Source/drain bottom diffusion smoothing parameter**	**-**	**0.3**	**-**
C_{sdesw}	**csdesw**	**Source/drain sidewall fringing capacitance per unit length**	**F/m**	**0.0**	**-**
CGSl	cgsl	Light doped source-gate region overlap capacitance	F/m	0.0	-
CGDl	cgdl	Light doped drain-gate region overlap capacitance	F/m	0.0	-
CKAPPA	ckappa	Coefficient for lightly doped region overlap capacitance fringing field capacitance	F/m	0.6	-
Cf	cf	Gate to source/drain fringing field capacitance	F/m	calcu-lated	**nC-6**
CLC	clc	Constant term for the short channel model	m	$0.1x10^{-7}$	-
CLE	cle	Exponential term for the short channel model	none	0.0	-
DLC	dlc	Length offset fitting parameter for gate charge	m	lint	-
DLCB	**dlcb**	**Length offset fitting parameter for body charge**	**m**	**0**	**-**
DLBG	**dlbg**	**Length offset fitting parameter for backgate charge**	**m**	**0.0**	**-**
DWC	dwc	Width offset fitting parameter from C-V	m	wint	-
DelVt	**delvt**	**Threshold voltage adjust for C-V**	**V**	**0.0**	**-**
F_{body}	**fbody**	**Scaling factor for body charge**	**-**	**1.0**	**-**
acde	**acde**	**Exponential coefficient for charge**	**m/V**	**1.0**	**-**

		thickness in capMod=3 for accumulation and depletion regions.			
moin	**moin**	**Coefficient for the gate-bias dependent surface potential.**	**$V^{1/2}$**	**15.0**	**-**

B.6. Temperature Parameters

Symbol used in equation	Symbol used in SPICE	Description	Unit	Default	Note
Tnom	tnom	Temperature at which parameters are expected	ºC	27	-
mte	ute	Mobility temperature exponent	none	-1.5	-
Kt1	kt1	Temperature coefficient for threshold voltage	V	-0.11	-
Kt11	kt11	Channel length dependence of the temperature coefficient for threshold voltage	V*m	0.0	
Kt2	kt2	Body-bias coefficient of the Vth temperature effect	none	0.022	-
Ua1	ua1	Temperature coefficient for U_a	m/V	4.31e-9	-
Ub2	ub1	Temperature coefficient for U_b	$(m/V)^2$	-7.61e-18	-
Uc1	uc1	Temperature coefficient for Uc	1/V	-.056	**nT-1**
At	at	Temperature coefficient for saturation velocity	m/sec	3.3e4	-
Tcijswg	**tcjswg**	**Temperature coefficient of C_{jswg}**	**1/K**	**0**	**-**
Tpbswg	**tpbswg**	**Temperature coefficient of P_{bswg}**	**V/K**	**0**	**-**
Cth0	**cth0**	**Normalized thermal capacity**	**(W*sec) / mºC**	**1e-5**	**-**
Prt	prt	Temperature coefficient for Rdsw	Ω-μm	0	-
Rth0	**rth0**	**Normalized thermal resistance**	**mºC/W**	**0**	**-**
Nt_{recf}	**Ntrecf**	**Temperature coefficient for N_{recf}**	**-**	**0**	**-**
Nt_{recr}	**Ntrecr**	**Temperature coefficient for N_{recr}**	**-**	**0**	**-**

X_{bjt}	**xbjt**	**Power dependence of j_{bjt} on temperature**	**-**	**1**	**-**
X_{dif}	**xdif**	**Power dependence of j_{dif} on temperature**	**-**	**X_{bjt}**	**-**
X_{rec}	**xrec**	**Power dependence of j_{rec} on temperature**	**-**	**1**	**-**
X_{tun}	**xtun**	**Power dependence of j_{tun} on temperature**	**-**	**0**	**-**
W_{th0}	**Wth0**	**Minimum width for thermal resistance calculation**	**m**	**0**	**-**

B.7. RF Model Parameters

Symbol used in equation	Symbol used in SPICE	Description	Unit	Default
RgateMod	rgateMod	Gate resistance model selector rgateMod = 0 No gate resistance rgateMod = 1 Constant gate resistance rgateMod = 2 Rii model with variable resistance rgateMod = 3 Rii model with two nodes	-	0
XRCRG1	xrcrg1	Parameter for distributed channel-resistance effect for intrinsic input resistance	-	12.0
XRCRG2	xrcrg2	Parameter to account for the excess channel diffusion resistance for intrinsic input resistance	-	1.0
NGCON	ngcon	Number of gate contacts	-	1
XGW	xgw	Distance from the gate contact to the channel edge	m	0.0
XGL	xgl	Offset of the gate length due to variations in patterning	m	0.0

B.8. Model Parameter Notes

nI-1. BSIMSOI supports *capmod*=2 and 3 only. *Capmod=0* and *1* are not supported.

nI-2. In modern SOI technology, source/drain extension or LDD are commonly used. As a result, the source/drain junction depth (X_j) can be different from the silicon film thickness (T_{si}). By default, if X_j is not given, it is set to T_{si}. X_j is not allowed to be greater than T_{si}.

nI-3. BSIMSOI refers substrate to the silicon below buried oxide, not the well region in BSIM3. It is used to calculate backgate flatband voltage (V_{fbb}) and parameters related to source/drain diffusion bottom capacitance (V_{sdth}, V_{sdfb}, C_{sdmin}). Positive n_{sub} means the same type of doping as the body and negative n_{sub} means opposite type of doping.

nC-1. If *cgso* is not given then it is calculated using:

if (*dlc* is given and is greater 0) then,

cgso = *p1* = (*dlc***cox*) - *cgs1*

if (the previously calculated *cgso* <0), then

cgso = 0

else *cgso* = 0.6 * *Tsi* * *cox*

nC-2. *Cgdo* is calculated in a way similar to *Csdo*

nC-3. If (n_{sub} is positive)

$$V_{sdfb} = -\frac{kT}{q}\log\left(\frac{10^{20}\cdot n_{sub}}{n_i \cdot n_i}\right) - 0.3$$

else

$$V_{sdfb} = -\frac{kT}{q}\log\left(\frac{10^{20}}{n_{sub}}\right) + 0.3$$

nC-4. If (n_{sub} is positive)

$$f_{sd} = 2\frac{kT}{q}\log\left(\frac{n_{sub}}{n_i}\right),\ g_{sd} = \frac{5.753\times10^{-12}\sqrt{n_{sub}}}{C_{box}}$$

$$V_{sdth} = V_{sdfb} + f_{sd} + g_{sd}\sqrt{f_{sd}}$$

else

$$f_{sd} = 2\frac{kT}{q}\log\left(-\frac{n_{sub}}{n_i}\right),\ g_{sd} = \frac{5.753\times10^{-12}\sqrt{-n_{sub}}}{C_{box}}$$

$$V_{sdth} = V_{sdfb} - f_{sd} - g_{sd}\sqrt{f_{sd}}$$

nC-5. $X_{sddep} = \sqrt{\frac{2e_{si}f_{sd}}{q\left|n_{sub}\cdot10^{6}\right|}}$, $C_{sddep} = \frac{e_{si}}{X_{sddep}}$, $C_{sd\,\min} = \frac{C_{sddep}C_{box}}{C_{sddep}+C_{box}}$

nC-6. If cf is not given then it is calculated using

$$CF = \frac{2e_{ox}}{p}\ln\left(1+\frac{4\times10^{-7}}{T_{ox}}\right)$$

nT-1. For mobmod=1 and 2, the unit is m/V^2. Default is -5.6E-11. For mobmod=3, unit is 1/V and default is -0.056.

Appendix C: Equation List

Equation List for BSIMSOI Built-In Potential Lowering Calculation

If SoiMod=0 (default), the model equation is identical to BSIMPD equation.

If SoiMod=1 (unified model for PD&FD) or SoiMod=2 (ideal FD), the following equations (FD module) are added on top of BSIMPD.

$$V_{bs0} = \frac{C_{Si}}{C_{Si}+C_{BOX}} \cdot \left(phi - \frac{qN_{ch}}{2e_{Si}} \cdot T_{Si}^{\ 2} + V_{nonideal} + \Delta V_{DIBL} \right) + h_e \frac{C_{BOX}}{C_{Si}+C_{BOX}} \cdot \left(V_{es} - V_{FBb} \right)$$

$$\text{where } C_{Si} = \frac{e_{Si}}{T_{Si}}, C_{BOX} = \frac{e_{OX}}{T_{BOX}}, C_{OX} = \frac{e_{OX}}{T_{OX}}$$

$$\Delta V_{DIBL} = D_{vbd0} \left(exp\left(- D_{vbd1} \frac{L_{eff}}{2l} \right) + 2exp\left(- D_{vbd1} \frac{L_{eff}}{l} \right) \right) \cdot \left(V_{bi} - 2\Phi_B \right)$$

$$h_e = K_{1b} - K_{2b} \cdot \left(exp\left(- D_{k2b} \frac{L_{eff}}{2l} \right) + 2exp\left(- D_{k2b} \frac{L_{eff}}{l} \right) \right)$$

$$phi = phi_{ON} - \frac{C_{OX}}{C_{OX} + \left(C_{Si}^{-1} + C_{BOX}^{-1} \right)^{-1}} \cdot N_{OFF,FD} V_t \cdot ln\left(1 + exp\left(\frac{V_{th,FD} - V_{gs\_eff} - V_{OFF,FD}}{N_{OFF,FD} V_t} \right) \right)$$

$$phi_{ON} = 2\Phi_B + V_t \, ln\left(1 + \frac{V_{gsteff.FD} \left(V_{gsteff,FD} + 2K1\sqrt{2\Phi_B} \right)}{MoinFD \cdot K1 \cdot V_t^{\ 2}} \right),$$

$$V_{gsteff,FD} = N_{OFF,FD} V_t \cdot ln\left(1 + exp\left(\frac{V_{gs\_eff} - V_{th,FD} - V_{OFF,FD}}{N_{OFF,FD} V_t} \right) \right)$$

Here Nch is the channel doping concentration. V_{FBb} is the backgate flatband voltage. $V_{th,FD}$ is the threshold voltage at $V_{bs}=V_{bs0}$(phi=$2\Phi_B$). V_t is thermal voltage. K1 is the body effect coefficient.

If SoiMod=1, the lower bound of V_{bs} (SPICE solution) is set to V_{bs0}. If SoiMod=2, V_{bs} is pinned at V_{bs0}. Notice that there is no body node and body leakage/charge calculation in SoiMod=2.

The zero field body potential that will determine the transistor threshold voltage, V_{bsmos}, is then calculated by

$$V_{bsmos} = V_{bs} - \frac{C_{Si}}{2qN_{ch}T_{Si}}\left(V_{bs0}\left(T_{OX} \to \infty\right) - V_{bs}\right)^2 \quad \text{if } V_{bs} \le V_{bs0}\left(T_{OX} \to \infty\right)$$
$$= V_{bs} \quad \text{else}$$

The subsequent clamping of V_{bsmos} will use the same equation that utilized in BSIMPD.

Equation List for BSIMSOI IV

Body Voltages

V_{bsh} is equal to the V_{bs} bounded between (V_{bsc}, f_{s1}). V_{bsh} is used in V_{th} and A_{bulk} calculation

$$T_1 = V_{bsc} + 0.5\left[V_{bs} - V_{bsc} - d + \sqrt{(V_{bs} - V_{bsc} - d)^2 - 4dV_{bsc}}\right],\ V_{bsc} = -5V$$

$$V_{bsh} = f_{s1} - 0.5\left[f_{s1} - T_1 - d + \sqrt{(f_{s1} - T_1 - d)^2 + 4dT_1}\right],\ f_{s1} = 1.5V$$

V_{bsh} is further limited to $0.95f_s$ to give V_{bseff}.

$$V_{bseff} = f_{s0} - 0.5\left[f_{s0} - V_{bsh} - d + \sqrt{(f_{s0} - V_{bsh} - d)^2 + 4dV_{bsh}}\right],\ f_{s0} = 0.95f_s$$

Effective Channel Length and Width

$$dW' = W_{\text{int}} + \frac{W_l}{L^{W_{\ln}}} + \frac{W_w}{W^{W_{wn}}} + \frac{W_{wl}}{L^{W_{\ln}} W^{W_{wn}}}$$

$$dW = dW' + dW_g V_{gsteff} + dW_b\left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right)$$

$$dL = L_{\text{int}} + \frac{L_l}{L^{L_{\ln}}} + \frac{L_w}{W^{L_{wn}}} + \frac{L_{wl}}{L^{L_{\ln}} W^{L_{wn}}}$$

$$L_{eff} = L_{drawn} - 2dL$$

$$W_{eff} = W_{drawn} - N_{bc}dW_{bc} - (2 - N_{bc})dW$$

$$W_{eff}' = W_{drawn} - N_{bc}dW_{bc} - (2 - N_{bc})dW'$$

$$W_{diod} = \frac{W_{eff}'}{N_{seg}} + P_{dbcp}$$

$$W_{dios} = \frac{W_{eff}'}{N_{seg}} + P_{sbcp}$$

Threshold Voltage

$$V_{th} = V_{tho} + K_{1eff}(sqrtPhisExt - \sqrt{\Phi_s}) - K_2 V_{bseff}$$
$$+ K_{1eff}(\sqrt{1 + \frac{N_{LX}}{L_{eff}}} - 1)\sqrt{\Phi_s} + (K_3 + K_{3b}V_{bseff})\frac{T_{ox}}{W_{eff}' + W_o}\Phi_s$$
$$- D_{VT0w}(\exp(-D_{VT1w}\frac{W_{eff}'L_{eff}}{2l_{tw}}) + 2\exp(-D_{VT1w}\frac{W_{eff}'L_{eff}}{l_{tw}}))(V_{bi} - \Phi_s)$$
$$- D_{VT0}(\exp(-D_{VT1}\frac{L_{eff}}{2l_t}) + 2\exp(-D_{VT1}\frac{L_{eff}}{l_t}))(V_{bi} - \Phi_s)$$
$$- (\exp(-D_{sub}\frac{L_{eff}}{2l_{to}}) + 2\exp(-D_{sub}\frac{L_{eff}}{l_{to}}))(E_{tao} + E_{tab}V_{bseff})V_{ds}$$

$$l_t = \sqrt{e_{si}X_{dep}/C_{ox}}(1 + D_{VT2}V_{bseff})$$

$$sqrtPhisExt = \sqrt{f_s - V_{bseff}} + s\left(V_{bsh} - V_{bseff}\right),\ s = -\frac{1}{2\sqrt{f_s - f_{s0}}}$$

$$K_{1eff} = K_1\left(1 + \frac{K_{1w1}}{W_{eff}' + K_{1w2}}\right)$$

$$l_{tw} = \sqrt{e_{si}X_{dep}/C_{ox}}(1 + D_{VT2w}V_{bseff}) \qquad l_{to} = \sqrt{e_{si}X_{dep0}/C_{ox}}$$

$$X_{dep} = \sqrt{\frac{2e_{si}(\Phi_s - V_{bseff})}{qN_{ch}}} \qquad X_{dep0} = \sqrt{\frac{2e_{si}\Phi_s}{qN_{ch}}}$$

$$V_{bi} = v_t \ln(\frac{N_{ch}N_{DS}}{n_i^2})$$

Poly depletion effect

$$V_{poly} + \frac{1}{2} X_{poly} E_{poly} = \frac{qN_{gate} X^2_{poly}}{2e_{si}}$$

$$e_{ox} E_{ox} = e_{si} E_{poly} = \sqrt{2qe_{si} N_{gate} V_{poly}}$$

$$V_{gs} - V_{FB} - f_x = V_{poly} + V_{ox}$$

$$a(V_{gs} - V_{FB} - f_s - V_{poly})^2 - V_{poly} = 0$$

$$a = \frac{e^2_{ox}}{2qe_{si} N_{gate} T^2_{ox}}$$

$$V_{gs\_eff} = V_{FB} + f_s + \frac{qe_{si} N_{gate} T^2_{ox}}{e^2_{ox}} \left[\sqrt{1 + \frac{2e^2_{ox} (V_{gs} - V_{FB} - f_s)}{qe_{si} N_{gate} T^2_{ox}}} - 1 \right]$$

Effective V_{gst} for all region (with Polysilicon Depletion Effect)

$$V_{gsteff} = \frac{2nv_t \ln\left[1 + \exp(\frac{V_{gs\_eff} - V_{th}}{2nv_t})\right]}{1 + 2nC_{ox}\sqrt{\frac{2\Phi_s}{qe_{si} N_{ch}}} \exp\left(-\frac{V_{gs\_eff} - V_{th} - 2V_{off}}{2nv_t}\right)}$$

$$n = 1 + N_{factor} \frac{e_{si} / X_{dep}}{C_{ox}} + \frac{(C_{dsc} + C_{dscd} V_{ds} + C_{dscb} V_{bseff}) \left[\exp(-D_{VT1} \frac{L_{eff}}{2l_t}) + 2\exp(-D_{VT1} \frac{L_{eff}}{l_t})\right]}{C_{ox}} + \frac{C_{it}}{C_{ox}}$$

Effective Bulk Charge Factor

$$A_{bulk} = 1 + \left(\frac{K_{1eff}}{2\sqrt{(f_s + Ketas) - \frac{V_{bsh}}{1 + Keta \cdot V_{bsh}}}} \left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{T_{si} X_{dep}}} \left(1 - A_{gs} V_{gsteff} \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{T_{si} X_{dep}}} \right)^2 \right) + \frac{B_0}{W'_{eff} + B_1} \right) \right)$$

$$A_{bulk0} = A_{bulk}\left(V_{gsteff} = 0\right)$$

Mobility and Saturation Velocity

For Mobmod=1

$$m_{eff} = \frac{m_o}{1 + (U_a + U_c V_{bseff})(\frac{V_{gsteff} + 2V_{th}}{T_{ox}}) + U_b(\frac{V_{gsteff} + 2V_{th}}{T_{ox}})^2}$$

For Mobmod=2

$$m_{eff} = \frac{m_o}{1 + (U_a + U_c V_{bseff})(\frac{V_{gsteff}}{T_{ox}}) + U_b(\frac{V_{gsteff}}{T_{ox}})^2}$$

For Mobmod=3

$$m_{eff} = \frac{m_0}{1 + [U_a(\frac{V_{gstef} + 2V_{th}}{T_{ox}}) + U_b(\frac{V_{gsteff} + 2V_{th}}{T_{ox}})^2](1 + U_c V_{bseff})}$$

Drain Saturation Voltage

For R_{ds}>0 or $\lambda \neq 1$:

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

$$a = A_{bulk}{}^2 W_{eff} n_{sat} C_{ox} R_{ds} + (\frac{1}{l} - 1) A_{bulk}$$

$$b = -\left[(V_{gsteff} + 2n_t)(\frac{2}{l} - 1) + A_{bulk} E_{sat} L_{eff} + 3A_{bulk}(V_{gsteff} + 2n_t) W_{eff} n_{sat} C_{ox} R_{ds} \right]$$

$$c = (V_{gsteff} + 2n_t) E_{sat} L_{eff} + 2(V_{gsteff} + 2n_t)^2 W_{eff} n_{sat} C_{ox} R_{ds}$$

$$l = A_1 V_{gsteff} + A_2$$

For R_{ds}=0, λ=1:

$$V_{dsat} = \frac{E_{sat} L_{eff} (V_{gsteff} + 2n_t)}{A_{bulk} E_{sat} L_{eff} + (V_{gsteff} + 2n_t)}$$

$$E_{sat} = \frac{2n_{sat}}{m_{eff}}$$

V_{dseff}

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left[V_{dsat} - V_{ds} - d + \sqrt{(V_{dsat} - V_{ds} - d)^2 + 4dV_{dsat}}\right]$$

Drain current expression

$$I_{ds,MOSFET} = \frac{1}{N_{seg}} \frac{I_{ds0}(V_{dseff})}{1 + \frac{R_{ds} I_{dso}(V_{dseff})}{V_{dseff}}} (1 + \frac{V_{ds} - V_{dseff}}{V_A})$$

$$b = m_{eff} C_{ox} \frac{W_{eff}}{L_{eff}}$$

$$I_{dso} = \frac{bV_{gsteff}\left(1 - A_{bulk} \frac{V_{dseff}}{2\left(V_{gsteff} + 2v_t\right)}\right)V_{dseff}}{1 + \frac{V_{dseff}}{E_{sat} L_{eff}}}$$

$$V_A = V_{Asat} + \left(1 + \frac{P_{vag} V_{gsteff}}{E_{sat} L_{eff}}\right)(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}})^{-1}$$

$$V_{ACLM} = \frac{A_{bulk} E_{sat} L_{eff} + V_{gsteff}}{P_{clm} A_{bulk} E_{sat} litl} (V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2n_t)}{q_{rout}(1 + P_{DIBLCB} V_{bseff})} (1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + 2n_t})$$

$$q_{rout} = P_{DIBLC1}[\exp(-D_{ROUT} \frac{L_{eff}}{2l_{t0}} + 2\exp(-D_{ROUT} \frac{L_{eff}}{l_{t0}})] + P_{DIBLC2}$$

$$V_{Asat} = \frac{E_{sat} L_{eff} + V_{dsat} + 2R_{ds} n_{sat} C_{ox} W_{eff} V_{gsteff} [1 - \frac{A_{bulk} V_{dsat}}{2(V_{gsteff} + 2n_t)}]}{2 / l - 1 + R_{ds} n_{sat} C_{ox} W_{eff} A_{bulk}}$$

$$litl = \sqrt{\frac{e_{si} T_{ox} T_{Si}}{e_{ox}}}$$

Drain/Source Resistance

$$R_{ds} = R_{dsw} \frac{1 + P_{rwg} V_{gsteff} + P_{rwb} \left(\sqrt{f_s - V_{bseff}} - \sqrt{f_s} \right)}{\left(10^6 W_{eff}^{'} \right)^{Wr}}$$

Impact Ionization Current

$$I_{ii} = a_0 (I_{ds,MOSFET} + F_{bjtii} I_c) \exp\left(\frac{V_{diff}}{b_2 + b_1 V_{diff} + b_0 V_{diff}^2} \right)$$

$$V_{diff} = V_{ds} - V_{dsatii}$$

$$V_{dsatii} = VgsStep + \left[V_{dsatii0} \left(1 + T_{ii} \left(\frac{T}{T_{nom}} - 1 \right) \right) - \frac{L_{ii}}{L_{eff}} \right]$$

$$VgsStep = \left(\frac{E_{satii} L_{eff}}{1 + E_{satii} L_{eff}} \right) \left(\frac{1}{1 + S_{ii1} V_{gsteff}} + S_{ii2} \right) \left(\frac{S_{ii0} V_{gst}}{1 + S_{iid} V_{ds}} \right)$$

Gate-Induced-Drain-Leakage (GIDL)

At drain, $I_{dgidl} = W_{diod} a_{gidl} E_s \exp\left(-\frac{b_{gidl}}{E_s}\right),\ E_s = \frac{V_{ds} - V_{gs} - c}{3T_{ox}}$

At source, $I_{sgidl} = W_{dios} a_{gidl} E_s \exp\left(-\frac{b_{gidl}}{E_s}\right),\ E_s = \frac{-V_{gs} - c}{3T_{ox}}$

If E_s is negative, I_{gidl} is set to zero for both drain and source.

Oxide tunneling current

In inversion,

$$J_{gb} = A\frac{V_{gb}V_{aux}}{T_{ox}^2}\left(\frac{\mathrm{T_{oxref}}}{T_{oxqm}}\right)^{\mathrm{N_{tox}}} exp\left(\frac{-B\left(\acute{a}_{\mathrm{gb1}} - \hat{a}_{\mathrm{gb1}}\left|V_{ox}\right|\right)T_{ox}}{1 - \left|V_{ox}\right|/\mathrm{V_{gb1}}}\right)$$

$$V_{aux} = \mathrm{V_{EVB}}\, ln\left(1 + exp\left(\frac{\left|V_{ox}\right| - \ddot{o}_{\mathrm{g}}}{\mathrm{V_{EVB}}}\right)\right)$$

$$A = \frac{q^3}{8phf_b}$$

$$B = \frac{8p\sqrt{2m_{ox}}f_b^{3/2}}{3hq}$$

$$f_b = 4.2eV$$

$$m_{ox} = 0.3m_0$$

In accumulation,

$$J_{gb} = A\frac{V_{gb}V_{aux}}{T_{ox}^2}\left(\frac{\mathrm{T_{oxref}}}{T_{oxqm}}\right)^{\mathrm{N_{tox}}} exp\left(\frac{-B\left(\acute{a}_{\mathrm{gb2}} - \hat{a}_{\mathrm{gb2}}\left|V_{ox}\right|\right)T_{ox}}{1 - \left|V_{ox}\right|/\mathrm{V_{gb2}}}\right)$$

$$V_{aux} = \mathrm{V_{ECB}}V_t\, ln\left(1 + exp\left(-\frac{V_{gb} - V_{fb}}{\mathrm{V_{ECB}}}\right)\right)$$

$$A = \frac{q^3}{8phf_b}$$

$$B = \frac{8p\sqrt{2m_{ox}}f_b^{3/2}}{3hq}$$

$$f_b = 3.1eV$$

$$m_{ox} = 0.4m_0$$

Body contact current

$$R_{bp} = \left(R_{body} \frac{W'_{eff} / N_{seg}}{L_{eff}} \right) \| \left(R_{halo} \frac{W'_{eff} / N_{seg}}{2} \right), \; R_{bodyext} = R_{bsh} N_{rb}$$

For 4-T device, $I_{bp} = 0$

For 5-T device,

$$I_{bp} = \frac{V_{bp}}{R_{bp} + R_{bodyext}}$$

Diode and BJT currents

Bipolar Transport Factor

$$a_{bjt} = \exp\left[-0.5 \left(\frac{L_{eff}}{L_n} \right)^2 \right]$$

Body-to-Source/drain diffusion

$$I_{bs1} = W_{dios} T_{si} j_{sdif} \left(\exp\left(\frac{V_{bs}}{n_{dio} V_t} \right) - 1 \right)$$

$$I_{bd1} = W_{diod} T_{si} j_{sdif} \left(\exp\left(\frac{V_{bd}}{n_{dio} V_t} \right) - 1 \right)$$

Recombination/trap-assisted tunneling current in depletion region

$$I_{bs2} = W_{dios} T_{si} j_{srec} \left(\exp\left(\frac{V_{bs}}{0.026 n_{recf}} \right) - \exp\left(\frac{V_{sb}}{0.026 n_{recr}} \frac{V_{rec0}}{V_{rec0} + V_{sb}} \right) \right)$$

$$I_{bd2} = W_{diod} T_{si} j_{srec} \left(\exp\left(\frac{V_{bd}}{0.026 n_{recf}} \right) - \exp\left(\frac{V_{db}}{0.026 n_{recr}} \frac{V_{rec0}}{V_{rec0} + V_{db}} \right) \right)$$

Reversed bias tunneling leakage

$$I_{bs4} = W_{dios} T_{si} j_{stun} \left(1 - exp\left(\frac{V_{sb}}{0.026 n_{tun}} \frac{V_{tun0}}{V_{tun0} + V_{sb}} \right) \right)$$

$$I_{bd4} = W_{diod} T_{si} j_{stun} \left(1 - exp\left(\frac{V_{db}}{0.026 n_{tun}} \frac{V_{tun0}}{V_{tun0} + V_{db}} \right) \right)$$

Recombination current in neutral body

$$I_{bs3} = \left(1 - a_{bjt}\right) I_{en} \left[\exp\left(\frac{V_{bs}}{n_{dio} V_t} \right) - 1 \right] \frac{1}{\sqrt{E_{hlis} + 1}}$$

$$I_{bd3} = \left(1 - a_{bjt}\right) I_{en} \left[\exp\left(\frac{V_{bd}}{n_{dio} V_t} \right) - 1 \right] \frac{1}{\sqrt{E_{hlid} + 1}}$$

$$I_{en} = \frac{W_{eff}^{'}}{N_{seg}} T_{si} j_{sbjt} \left[L_{bjt0} \left(\frac{1}{L_{eff}} + \frac{1}{L_n} \right) \right]^{N_{bjt}}$$

$$E_{hlis} = A_{hli\_eff} \left[\exp\left(\frac{V_{bs}}{n_{dio} V_t} \right) - 1 \right]$$

$$E_{hlid} = A_{hli\_eff} \left[\exp\left(\frac{V_{bd}}{n_{dio} V_t} \right) - 1 \right]$$

$$A_{hli\_eff} = A_{hli} \exp\left[\frac{-E_g(300K)}{n_{dio} V_t} X_{bjt} \left(1 - \frac{T}{T_{nom}} \right) \right]$$

BJT collector current

$$I_c = a_{bjt} I_{en} \left\{ \exp\left[\frac{V_{bs}}{n_{dio} V_t} \right] - \exp\left[\frac{V_{bd}}{n_{dio} V_t} \right] \right\} \frac{1}{E_{2nd}}$$

$$E_{2nd} = \frac{E_{ely} + \sqrt{E_{ely}^{\ 2} + 4E_{hli}}}{2}$$

$$E_{ely} = 1 + \frac{V_{bs} + V_{bd}}{V_{Abjt} + A_{ely} L_{eff}}$$

$$E_{hli} = E_{hlis} + E_{hlid}$$

Total body-source/drain current

$$I_{bs} = I_{bs1} + I_{bs2} + I_{bs3} + I_{bs4}$$

$$I_{bd} = I_{bd1} + I_{bd2} + I_{bd3} + I_{bd4}$$

Total body current

$$I_{ii} + I_{dgidl} + I_{sgidl} + I_{gb} - I_{bs} - I_{bd} - I_{bp} = 0$$

Temperature effects

$$V_{th(T)} = V_{th(Tnom)} + (K_{T1} + K_{t1l} / L_{eff} + K_{T2} V_{bseff})(T / T_{nom} - 1)$$

$$m_{o(T)} = m_{o(Tnom)} \left(\frac{T}{T_{nom}}\right)^{mte}, \quad n_{sat(T)} = n_{sat(Tnom)} - A_T (T / T_{nom} - 1)$$

$$R_{dsw(T)} = R_{dsw(} T_{nom)} + P_{rt} \left(\frac{T}{T_{nom}} - 1\right)$$

$$U_{a(T)} = U_{a(Tnom)} + U_{a1} (T / T_{nom} - 1)$$

$$U_{b(T)} = U_{b(Tnom)} + U_{b1} (T / T_{nom} - 1)$$

$$U_{c(T)} = U_{c(Tnom)} + U_{c1} (T / T_{nom} - 1)$$

$$R_{th} = \frac{R_{th0}}{\left(W_{eff}^{'} + W_{th0}\right)/N_{seg}}\ ,\ C_{th} = C_{th0}\,\frac{W_{eff}^{'} + W_{th0}}{N_{seg}}$$

$$j_{sbjt} = j_{sbjt0}\exp\left[\frac{-E_g(300K)}{n_{dio}V_t}X_{bjt}\left(1-\frac{T}{T_{nom}}\right)\right]$$

$$j_{sdif} = j_{sdif0}\exp\left[\frac{-E_g(300K)}{n_{dio}V_t}X_{dif}\left(1-\frac{T}{T_{nom}}\right)\right]$$

$$j_{srec} = j_{srec0}\exp\left[\frac{-E_g(300K)}{n_{recf0}V_t}X_{rec}\left(1-\frac{T}{T_{nom}}\right)\right]$$

$$j_{stun} = j_{stun0}\exp\left[X_{tun}\left(\frac{T}{T_{nom}}-1\right)\right]$$

$$n_{recf} = n_{recf0}\left[1+nt_{recf}\left(\frac{T}{T_{nom}}-1\right)\right]$$

$$n_{recr} = n_{recr0}\left[1+nt_{recr}\left(\frac{T}{T_{nom}}-1\right)\right]$$

E_g is the energy gap energy.

Gate-to-channel current (Igc) and gate-to-S/D current (Igs and Igd)

Igc –gate to channel tunneling current

$$Igc = W_{eff}\,L_{eff}\cdot A\cdot T_{oxRatio}\cdot V_{gs\_eff}\cdot V_{aux}\cdot\exp\left[-B\cdot T_{oxqm}\left(aigc - bigc\cdot V_{oxdepinv}\right)\cdot\left(1+cigc\cdot V_{oxdepinv}\right)\right]$$

Note here *Igc* **is the gate to channel current with Vds=0**

$$V_{aux} = nigc\cdot V_m\cdot\log\left(1+\exp\left(\frac{V_{gs\_eff}-V_{th0}}{nigc\cdot V_{tm}}\right)\right)$$

$$T_{oxRatio} = \left(\frac{T_{oxref}}{T_{oxqm}} \right)^{ntox} \cdot \frac{1}{T_{oxqm}^2}$$

Igs and Igd –gate tunneling current between the gate and the source/drain diffusion region

$$Igs = W_{eff}\, Dlcig \cdot A \cdot T_{oxRatioEdg} \cdot V_{gs} \cdot V'_{gs} \cdot \exp\left[- B \cdot T_{oxqm} \cdot Poxedge \cdot \left(aigsd - bigsd \cdot V'_{gs} \right) \cdot \left(1 + cigsd \cdot V'_{gs} \right) \right]$$

$$Igd = W_{eff}\, Dlcig \cdot A \cdot T_{oxRatioEdg} \cdot V_{gd} \cdot V'_{gd} \cdot \exp\left[- B \cdot T_{oxqm} \cdot Poxedge \cdot \left(aigsd - bigsd \cdot V'_{gd} \right) \cdot \left(1 + cigsd \cdot V'_{gd} \right) \right.$$

$$T_{oxRatioEdge} = \left(\frac{T_{oxref}}{T_{oxqm} \cdot Poxedge} \right)^{ntox} \cdot \frac{1}{\left(T_{oxqm} \cdot Poxedge \right)^2}$$

$V'_{gs} = \sqrt{\left(V_{gs} - V_{fbsd} \right)^2 + 1.0e-4}$, $V'_{gd} = \sqrt{\left(V_{gd} - V_{fbsd} \right)^2 + 1.0e-4}$.

Partition of Igc

$$Igc = Igcs + I\,\mathrm{gcd}$$

$$Igcs = Igc \cdot \frac{pi\,\mathrm{gcd} \cdot V_{ds} + \exp\left(- pi\,\mathrm{gcd} \cdot V_{ds} \right) - 1 + 1.0e-4}{pi\,\mathrm{gcd}^2 \cdot V_{ds}^2 + 2.0e-4}$$

$$I\,\mathrm{gcd} = Igc \cdot \frac{1 - \left(pi\,\mathrm{gcd} \cdot V_{ds} + 1 \right) \cdot \exp\left(- pi\,\mathrm{gcd} \cdot V_{ds} \right) + 1.0e-4}{pi\,\mathrm{gcd}^2 \cdot V_{ds}^2 + 2.0e-4}$$

Equation List for BSIMSOI CV

Dimension Dependence

$$dW_{eff} = DWC + \frac{W_{lc}}{L^{W_{ln}}} + \frac{W_{wc}}{W^{W_{wn}}} + \frac{W_{wlc}}{L^{W_{ln}} W^{W_{wn}}}$$

$$dL_{eff} = DLC + \frac{L_{lc}}{L^{L_{ln}}} + \frac{L_{wc}}{W^{L_{wn}}} + \frac{L_{wlc}}{L^{L_{ln}} W^{L_{wn}}}$$

$$L_{active} = L_{drawn} - 2dL_{eff}$$
$$L_{activeB} = L_{active} - DLCB$$
$$L_{activeBG} = L_{activeB} + 2dL_{bg}$$

$$W_{active} = W_{drawn} - N_{bc} dW_{bc} - (2 - N_{bc}) dW_{eff}$$
$$W_{diosCV} = \frac{W_{active}}{N_{seg}} + P_{sbcp}$$
$$W_{diodCV} = \frac{W_{active}}{N_{seg}} + P_{dbcp}$$

Charge Conservation

$$Q_{Bf} = Q_{acc} + Q_{sub0} + Q_{subs}$$

$$Q_{inv} = Q_{inv,s} + Q_{inv,d}$$

$$Q_g = -\left(Q_{inv} + Q_{Bf}\right)$$

$$Q_b = Q_{Bf} - Q_e + Q_{js} + Q_{jd}$$

$$Q_s = Q_{inv,s} - Q_{js}$$

$$Q_d = Q_{inv,d} - Q_{jd}$$

$$Q_g + Q_e + Q_b + Q_s + Q_d = 0$$

Intrinsic Charges

(1) capMod = 2

Front Gate Body Charge

Accumulation Charge

$$V_{FBeff} = V_{fb} - 0.5\left(\left(V_{fb} - V_{gb} - d\right) + \sqrt{\left(V_{fb} - V_{gb} - d\right)^2 + d^2} \right)$$

where $V_{gb} = V_{gs} - V_{bseff}$

$$V_{fb} = V_{th} - f_s - K_{1eff}\sqrt{f_s - V_{bseff}} + delvt$$

$$V_{gsteffCV} = nv_t \ln\left(1 + \exp\left[\frac{V_{gs} - V_{th}}{nv_t}\right] \cdot \exp\left[-\frac{delvt}{nv_t}\right]\right)$$

$$Q_{acc} = -F_{body}\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{ox}(V_{FBeff} - V_{fb})$$

Gate Induced Depletion Charge

$$Q_{sub0} = -F_{body}\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{ox}\frac{K_{1eff}^{\ 2}}{2}\left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FBeff} - V_{gsteffCV} - V_{bseff})}{K_{1eff}^{\ 2}}}\right)$$

Drain Induced Depletion Charge

$$V_{dsatCV} = V_{gsteffCV} / A_{bulkCV},\ A_{bulkCV} = A_{bulk0}\left[1 + \left(\frac{CLC}{L_{activeB}}\right)^{CLE}\right]$$

$$V_{dsCV} = V_{dsatCV} - \frac{1}{2}(V_{dsatCV} - V_{ds} - d + \sqrt{(V_{dsatCV} - V_{ds} - d)^2 + 4d\ V_{dsatCV}})$$

$$Q_{subs} = F_{body}\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{ox}\left(A_{bulkCV} - 1\right)\left[\frac{V_{dsCV}}{2} - \frac{A_{bulkCV}V_{dsCV}^{2}}{12\left(V_{gsteffCV} - A_{bulkCV}V_{dsCV}/2\right)}\right]$$

Back Gate Body Charge

$$Q_e = k_{b1}F_{body}\left(\frac{W_{active}L_{activeBG}}{N_{seg}} + A_{ebcp}\right)C_{box}\left(V_{es} - V_{fbb} - V_{bseff}\right)$$

Inversion Charge

$$V_{cveff} = V_{dsat,CV} - 0.5\left(V_4 + \sqrt{V_4^{2} + 4d_4V_{dsat,CV}}\right) where V_4 = V_{dsat,CV} - V_{ds} - d_4; d_4 = 0.02$$

$$Q_{inv} = -\left(\frac{W_{active}L_{active}}{N_{seg}} + A_{gbcp}\right)C_{ox}\left(\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff}\right) + \frac{A_{bulkCV}{}^{2}V_{cveff}{}^{2}}{12\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff}\right)}\right)$$

50/50 Charge Partition

$$Q_{inv,s} = Q_{inv,.d} = 0.5Q_{inv}$$

40/60 Charge Partition

$$Q_{inv,s} = -\frac{\left(\frac{W_{active}L_{active}}{N_{seg}} + A_{gbcp}\right)C_{ox}}{2\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cvefff}\right)^{2}}\left(V_{gsteffCV}{}^{3} - \frac{4}{3}V_{gsteffCV}{}^{2}\left(A_{bulkCV}V_{cveff}\right) + \frac{2}{3}V_{gsteff}\left(A_{bulkCV}V_{cveff}\right)^{2} - \frac{2}{15}\left(A_{bulkCV}V_{cveff}\right)^{3}\right)$$

$$Q_{inv,d} = -\frac{\left(\frac{W_{active}L_{active}}{N_{seg}} + A_{gbcp}\right)C_{ox}}{2\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cvefff}\right)^{2}}\left(V_{gsteffCV}{}^{3} - \frac{5}{3}V_{gsteffCV}{}^{2}\left(A_{bulkCV}V_{cveff}\right) + V_{gsteff}\left(A_{bulkCV}V_{cveff}\right)^{2} - \frac{1}{5}\left(A_{bulkCV}V_{cveff}\right)^{3}\right)$$

0/100 Charge Partition

$$Q_{inv,s} = -\frac{W_{active}L_{active} + A_{gbcp}}{N_{seg}} C_{ox}\left(\frac{V_{gsteffCV}}{2} + \frac{A_{bulkCV}V_{cveff}}{4} - \frac{\left(A_{bulkCV}V_{cveff}\right)^2}{24\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff}\right)}\right)$$

$$Q_{inv,d} = -\frac{W_{active}L_{active} + A_{gbcp}}{N_{seg}} C_{ox}\left(\frac{V_{gsteffCV}}{2} - \frac{3A_{bulkCV}V_{cveff}}{4} + \frac{\left(A_{bulkCV}V_{cveff}\right)^2}{8\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff}\right)}\right)$$

(2) capMod = 3 (Charge-Thickness Model)

capMod = 3 only supports zero-bias flat band voltage, which is calculated from bias-independent threshold voltage. This is different from capMod = 2. For the finite thickness (X_{DC}) formulation, refer to Chapter 4 of BSIM3v3.2 Users's Manual.

Front Gate Body Charge

Accumulation Charge

$$V_{FBeff} = V_{fb} - 0.5\left(\left(V_{fb} - V_{gb} - d\right) + \sqrt{\left(V_{fb} - V_{gb} - d\right)^2 + d^2}\right)$$

where $V_{gb} = V_{gs} - V_{bseff}$

$$V_{fb} = V_{th} - f_s - K_{1eff}\sqrt{f_s - V_{bseff}}$$

$$Q_{acc} = -F_{body}\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{oxeff}V_{gbacc}$$

$$V_{gbacc} = 0.5\left(V_0 + \sqrt{V_0^2 + 4dV_{fb}}\right)$$

$$V_0 = V_{fb} + V_{bseff} - V_{gs} - d$$

$$C_{oxeff} = \frac{C_{ox}C_{cen}}{C_{ox} + C_{cen}}$$

$$C_{cen} = e_{Si} / X_{DC}$$

Gate Induced Depletion Charge

$$Q_{sub0} = -F_{body}\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{oxeff}\frac{K_{1eff}^{\ 2}}{2}\left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FBeff} - V_{gsteffCV} - V_{bseff})}{K_{1eff}^{\ 2}}}\right)$$

Drain Induced Depletion Charge

$$V_{dsatCV} = \left(V_{gsteffCV} - \Phi_d\right) / A_{bulkCV}$$

$$\Phi_d = \Phi_s - 2\Phi_B = v_t \ln\left[1 + \frac{V_{gsteffCV}\left(V_{gstefCV} + 2K_{1eff}\sqrt{2\Phi_B}\right)}{moinK_{1eff}v_t^2}\right]$$

$$V_{dsCV} = V_{dsatCV} - \frac{1}{2}(V_{dsatCV} - V_{ds} - d + \sqrt{(V_{dsatCV} - V_{ds} - d)^2 + 4d\ V_{dsatCV}})$$

$$Q_{subs} = F_{body}\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{oxeff}\left(A_{bulkCV} - 1\right)\left[\frac{V_{dsCV}}{2} - \frac{A_{bulkCV}V_{dsCV}^2}{12\left(V_{gsteffCV} - \Phi_d - A_{bulkCV}V_{dsCV}/2\right)}\right]$$

Back Gate Body Charge

$$Q_e = k_{b1} F_{body} \left(\frac{W_{active} L_{activeBG}}{N_{seg}} + A_{ebcp} \right) C_{box} \left(V_{es} - V_{fbb} - V_{bseff} \right)$$

Inversion Charge

$$V_{cveff} = V_{dsat,CV} - 0.5\left(V_4 + \sqrt{V_4^2 + 4d_4 V_{dsat,CV}}\right) where V_4 = V_{dsat,CV} - V_{ds} - d_4 ; d_4 = 0.02$$

$$Q_{inv} = -\left(\frac{W_{active} L_{active}}{N_{seg}} + A_{gbcp} \right) C_{oxeff} \left(\left(V_{gsteffCV} - \Phi_d - \frac{A_{bulkCV}}{2} V_{cveff} \right) + \frac{{A_{bulkCV}}^2 {V_{cveff}}^2}{12\left(V_{gsteffCV} - \Phi_d - \frac{A_{bulkCV}}{2} V_{cveff} \right)} \right)$$

50/50 Charge Partition

$$Q_{inv,s} = Q_{inv,.d} = 0.5 Q_{inv}$$

40/60 Charge Partition

$$Q_{inv,s} = -\frac{\left(\frac{W_{active} L_{active}}{N_{seg}} + A_{gbcp} \right) C_{oxeff}}{2\left(V_{gsteffCV} - \Phi_d - \frac{A_{bulkCV}}{2} V_{cvefff} \right)^2} \left(\left(V_{gsteffCV} - \Phi_d \right)^3 - \frac{4}{3}\left(V_{gsteffCV} - \Phi_d \right)^2 \left(A_{bulkCV} V_{cveff} \right) + \frac{2}{3}\left(V_{gsteff} - \Phi_d \right)\left(A_{bulkCV} V_{cveff} \right)^2 - \frac{2}{15}\left(A_{bulkCV} V_{cveff} \right.$$

$$Q_{inv,d} = -\frac{\left(\frac{W_{active} L_{active}}{N_{seg}} + A_{gbcp} \right) C_{oxef}}{2\left(V_{gsteffCV} - \Phi_d - \frac{A_{bulkCV}}{2} V_{cvefff} \right)^2} \left(\left(V_{gsteffCV} - \Phi_d \right)^3 - \frac{5}{3}\left(V_{gsteffCV} - \Phi_d \right)^2 \left(A_{bulkCV} V_{cveff} \right) + \left(V_{gstefCVf} - \Phi_d \right)\left(A_{bulkCV} V_{cveff} \right)^2 - \frac{1}{5}\left(A_{bulkCV} V_{cveff} \right)^3 \right.$$

0/100 Charge Partition

$$Q_{inv,s} = -\frac{W_{active}L_{active} + A_{gbcp}}{N_{seg}} C_{oxeff}\left(\frac{V_{gsteffCV} - \Phi_d}{2} + \frac{A_{bulkCV}V_{cveff}}{4} - \frac{\left(A_{bulkCV}V_{cveff}\right)^2}{24\left(V_{gsteffCV} - \Phi_d - \frac{A_{bulkCV}}{2}V_{cveff}\right)}\right)$$

$$Q_{inv,d} = -\frac{W_{active}L_{active} + A_{gbcp}}{N_{seg}} C_{oxeff}\left(\frac{V_{gsteffCV} - \Phi_d}{2} - \frac{3A_{bulkCV}V_{cveff}}{4} + \frac{\left(A_{bulkCV}V_{cveff}\right)^2}{8\left(V_{gsteffCV} - \Phi_d - \frac{A_{bulkCV}}{2}V_{cveff}\right)}\right)$$

Overlap Capacitance

Source Overlap Charge

$$V_{gs\_overlap} = \frac{1}{2}\left\{\left(V_{gs} + d\right) + \sqrt{\left(V_{gs} + d\right)^2 + 4d}\right\}$$

$$\frac{Q_{overlap,s}}{W_{diosCV}} = CGS0 \cdot V_{gs} + CGS1\left\{V_{gs} - V_{gs\_overlap} + \frac{CKAPPA}{2}\left(-1 + \sqrt{1 + \frac{4V_{gs\_overlap}}{CKAPPA}}\right)\right\}$$

Drain Overlap Charge

$$V_{gd\_overlap} = \frac{1}{2}\left\{\left(V_{gd} + d\right) + \sqrt{\left(V_{gd} + d\right)^2 + 4d}\right\}$$

$$\frac{Q_{overlap,d}}{W_{diodCV}} = CGD0 \cdot V_{gd} + CGD1\left\{V_{gd} - V_{gd\_overlap} + \frac{CKAPPA}{2}\left(-1 + \sqrt{1 + \frac{4V_{gd\_overlap}}{CKAPPA}}\right)\right\}$$

Gate Overlap Charge

$$Q_{overlap,g} = -\left(Q_{overlap,s} + Q_{overlap,d}\right)$$

Source/Drain Junction Charge

For $V_{bs} < 0.95 f_s$

$$Q_{jswg} = Q_{bsdep} + Q_{bsdif}$$

else

$$Q_{jswg} = C_{bsdep}(0.95 f_s)(V_{bs} - 0.95 f_s) + Q_{bsdif}$$

For $V_{bd} < 0.95 f_s$

$$Q_{jdwg} = Q_{bddep} + Q_{bddif}$$

else

$$Q_{jdwg} = C_{bddep}(0.95 f_s)(V_{bd} - 0.95 f_s) + Q_{bddif}$$

where

$$Q_{bsdep} = W_{diosCV} C_{jswg} \frac{T_{si}}{10^{-7}} \frac{P_{bswg}}{1 - Mj_{swg}} \left[1 - \left(1 - \frac{V_{bs}}{P_{bswg}} \right)^{1 - M_{jswg}} \right]$$

$$Q_{bddep} = W_{diodCV} C_{jswg} \frac{T_{si}}{10^{-7}} \frac{P_{bswg}}{1 - Mj_{swg}} \left[1 - \left(1 - \frac{V_{bd}}{P_{bswg}} \right)^{1 - M_{jswg}} \right]$$

$$Q_{bsdif} = t \frac{W_{eff}'}{N_{seg}} T_{si} J_{sbjt} \left[1 + L_{dif0} \left(L_{bj0} \left(\frac{1}{L_{eff}} + \frac{1}{L_n} \right)^{N_{dif}} \right) \right] \left[exp\left(\frac{V_{bs}}{n_{dio} V_t} \right) - 1 \right] \frac{1}{\sqrt{E_{hlis} + 1}}$$

$$Q_{bddif} = t \frac{W_{eff}'}{N_{seg}} T_{si} J_{sbjt} \left[1 + L_{dif0} \left(L_{bj0} \left(\frac{1}{L_{eff}} + \frac{1}{L_n} \right)^{N_{dif}} \right) \right] \left[exp\left(\frac{V_{bd}}{n_{dio} V_t} \right) - 1 \right] \frac{1}{\sqrt{E_{hlid} + 1}}$$

$$C_{jswg} = C_{jswg0} \left[1 + t_{cjswg} (T - T_{nom}) \right]$$

$$P_{bswg} = P_{bswg0} - t_{pbswg} (T - T_{nom})$$

Extrinsic Capacitance

Bottom S/D to Substrate Capacitance (per unit area)

$$C_{esb} = \begin{cases} C_{box} & \textit{if} \quad V_{s/d,e} < V_{sdfb} \\ C_{box} - \dfrac{1}{A_{sd}}(C_{box} - C_{min})\left(\dfrac{V_{s/d,e} - V_{sdfb}}{V_{sdth} - V_{sdfb}}\right)^2 & \textit{elseif} \quad V_{s/d,e} < V_{sdfb} + A_{sd}(V_{sdth} - V_{sdfb}) \\ C_{min} + \dfrac{1}{1 - A_{sd}}(C_{box} - C_{min})\left(\dfrac{V_{s/d,e} - V_{sdth}}{V_{sdth} - V_{sdfb}}\right)^2 & \textit{elseif} \quad V_{s/d,e} < V_{sdth} \\ C_{min} & \textit{else} \end{cases}$$

Sidewall S/D to Substrate Capacitance (per unit length)

$$C_{s/d,esw} = C_{sdesw} \log\left(1 + \frac{T_{si}}{T_{box}}\right)$$

Appendix D: Parameter Extraction

D.1. Extraction Strategy

The complicated physics in SOI MOSFETs makes parameter extraction quite involved [20]. It is always preferable to have more measurements so that the parameters extracted can have more valid physical meaning. Similar to conventional bulk devices, two basic extraction strategies can be used: single device extraction, and group device extraction. The group device extraction is more popular because of several reasons. In analog circuit, channel length and width scalability is very important. In digital circuit, statistical modeling is often used to predict the circuit performance due to process variation. Hence channel length scalability is also important. Besides, model parameters extracted from group device extraction have better physical meaning than that from single device extraction. In this work, we shall emphasize on group device extraction.

Parameter extraction using body contact devices is highly recommended because parameters related to body effect, impact ionization and leakage currents can be directly extracted [18, 19]. This yields less ambiguity in extracting technology parameters for I-V fitting purposes. In the followings, we suggest a set of measurement suitable for PD devices.

D.2. Suggested I-V Measurement

Measurement set A is used to extract basic MOS I-V parameters. For each body-contacted device :

(A1) I_{ds} vs. V_{gs} @ small V_{ds} with different V_{bs}, V_{es}=0V.

(A2) I_{ds} vs. V_{gs} @ V_{ds}=V_{dd} with different V_{bs}, V_{es}=0V.

(A3) I_{ds} vs. V_{ds} with different V_{gs} and different V_{bs}, V_{es}=0V.

Parameters extracted include threshold voltage, body coefficient, delta L and W, series resistance, mobility, short channel effect, and subthreshold swing. (A2) is used to extract DIBL parameters at subthreshold. (A3) is used to extract saturation velocity, body charge effect, output resistance, body contact resistance and self-heating parameters.

Measurement set C is used to extract impact ionization current parameters. For each body-contacted device :

(C1) I_b vs. V_{gs} @ different V_{ds}, V_{bs}=0V, V_{es}=0V.

(C2) I_b vs. V_{ds} @ different V_{gs}, V_{bs}=0V, V_{es}=0V.

Measurement set D is used to extract MOS temperature dependent parameter. For a long channel body-contacted device:

(D1) I_{ds} vs. V_{gs} @ small V_{ds}, V_{bs}=0V, V_{es}=0V, repeat with several temperatures.

(D2) I_{ds} vs. V_{ds} @ different V_{gs}, V_{bs}=0V, V_{es}=0V, repeat with several temperatures.

Notice that the self-heating parameters have to be extracted from set A.

Measurement set E is used to extract diode parameters. For a long channel body-contacted device or gated diode :

(E1) I_{diode} vs. V_{bs} @ V_{gs}=-1V, V_{es}=0V, repeat with several temperature

Measurement set F is used to extract BJT parameters. For each body-contacted device:

(F1) I_{ds} vs. I_b @ V_{gs}=-1V, V_{es}=0V, V_{ds}=1V.

Measurement set G is used to verify the floating body device data. For each floating-body device :

(G1) I_{ds} vs. V_{gs} @ small V_{ds}.

(G2) I_{ds} vs. V_{gs} @ V_{ds}=V_{dd}.

(G3) I_{ds} vs. V_{ds} @ different V_{gs}.

Appendix E: Model Parameter Binning

Below is the information on parameter binning regarding which model parameters can or cannot be binned. All those parameters which can be binned follow this implementation:

$$P = P_0 + \frac{P_L}{L_{eff}} + \frac{P_W}{W_{eff}} + \frac{P_P}{L_{eff} \times W_{eff}}$$

For example, for the parameter k1: P_0 = k1, P_L = lk1, P_W = wk1, P_P = pk1. binUnit is a bining unit selector. If binUnit = 1, the units of L_{eff} and W_{eff} used in the binning equation above have the units of microns; therwise in meters.

For example, for a device with L_{eff} = 0.5μm and W_{eff} = 10μm. If binUnit = 1, the parameter values for *vsat* are 1e5, 1e4, 2e4, and 3e4 for *vsat*, *lvsat*, *wvsat*, and *pvsat*, respectively. Therefore, the effective value of *vsat* for this device is

vsat = 1e5 + 1e4/0.5 + 2e4/10 + 3e4/(0.5*10) = 1.28e5

To get the same effective value of *vsat* for binUnit = 0, the values of *vsat*, *lvsat*, *wvsat*, and *pvsat* would be 1e5, 1e-2, 2e-2, 3e-8, respectively. Thus,

vsat = 1e5 + 1e-2/0.5e6 + 2e-2/10e-6 + 3e-8/(0.5e-6 * 10e-6) = 1.28e5

Model parameters that have been binned in BSIMPD2.1 are listed as follows:

E.1. DC Parameters

Symbol used in equation	Symbol used in SPICE	Description
V_{th0}	vth0	Threshold voltage @V_{bs}=0 for long and wide device
K_1	k1	First order body effect coefficient
$\boldsymbol{K_{1w1}}$	**k1w1**	**First body effect width dependent parameter**
$\boldsymbol{K_{1w2}}$	**k1w2**	**Second body effect width dependent parameter**
K_2	k2	Second order body effect coefficient
K_3	k3	Narrow width coefficient
K_{3b}	k3b	Body effect coefficient of k3
K_{b1}	Kb1	Backgate body charge coefficient
W_0	w0	Narrow width parameter
N_{LX}	nlx	Lateral non-uniform doping parameter
D_{vt0}	Dvt0	first coefficient of short-channel effect on Vth
D_{vt1}	dvt1	Second coefficient of short-channel effect on Vth
D_{vt2}	dvt2	Body-bias coefficient of short-channel effect on Vth
D_{vt0w}	dvt0w	first coefficient of narrow width effect on Vth for small channel length
D_{vt1w}	dvt1w	Second coefficient of narrow width effect on Vth for small channel length
D_{vt2w}	dvt2w	Body-bias coefficient of narrow width effect on Vth for small channel length
m_0	u0	Mobility at Temp = Tnom
U_a	ua	First-order mobility degradation coefficient
U_b	ub	Second-order mobility degradation coefficient
U_c	uc	Body-effect of mobility degradation coefficient
v_{sat}	vsat	Saturation velocity at Temp=Tnom
$A0$	a0	Bulk charge effect coefficient for channel length

A_{gs}	ags	Gate bias coefficient of A_{bulk}
B0	b0	Bulk charge effect coefficient for channel width
B1	b1	Bulk charge effect width offset
Keta	keta	Body-bias coefficient of bulk charge effect
Ketas	**Ketas**	**Surface potential adjustment for bulk charge effect**
A_1	A1	First non-saturation effect parameter
A_2	A2	Second non-saturation effect parameter
R_{dsw}	rdsw	Parasitic resistance per unit width
Prwb	prwb	Body effect coefficient of Rdsw
Prwg	prwg	Gate bias effect coefficient of Rdsw
Wr	wr	Width offset from Weff for Rds calculation
Nfactor	nfactor	Subthreshold swing factor
Wint	wint	Width offset fitting parameter from I-V without bias
Lint	lint	Length offset fitting parameter from I-V without bias
DWg	dwg	Coefficient of W_{eff}'s gate dependence
DWb	dwb	Coefficient of W_{eff}'s substrate body bias dependence
V_{off}	voff	Offset voltage in the subthreshold region for large W and L
Eta0	eta0	DIBL coefficient in subthreshold region
Etab	etab	Body-bias coefficient for the subthreshold DIBL effect
D_{sub}	dsub	DIBL coefficient exponent
C_{it}	cit	Interface trap capacitance
C_{dsc}	cdsc	Drain/Source to channel coupling capacitance
C_{dscb}	cdscb	Body-bias sensitivty of C_{dsc}
C_{dscd}	cdscd	Drain-bias sensitivty of C_{dsc}
P_{clm}	pclm	Channel length modulation parameter
P_{dibl1}	pdibl1	First output resistance DIBL effect correction parameter
P_{dibl2}	pdibl2	Second output resistance DIBL effect correction parameter
D_{rout}	drout	L dependence coefficient of the DIBL correction parameter in Rout
Pvag	pvag	Gate dependence of Early voltage

d	delta	Effective V_{ds} parameter
a_0	alpha0	The first parameter of impact ionization current
F_{bjtii}	**fbjtii**	**Fraction of bipolar current affecting the impact ionization**
b_0	**beta0**	**First V_{ds} dependent parameter of impact ionization current**
b_1	**beta1**	**Second V_{ds} dependent parameter of impact ionization current**
b_2	**beta2**	**Third V_{ds} dependent parameter of impact ionization current**
$V_{dsatii0}$	**vdsatii0**	**Nominal drain saturation voltage at threshold for impact ionization current**
T_{ii}	**tii**	**Temperature dependent parameter for impact ionization current**
L_{ii}	**lii**	**Channel length dependent parameter at threshold for impact ionization current**
E_{satii}	**esatii**	**Saturation channel electric field for impact ionization current**
S_{ii0}	**sii0**	**First V_{gs} dependent parameter for impact ionization current**
S_{ii1}	**sii1**	**Second V_{gs} dependent parameter for impact ionization current**
S_{ii2}	**sii2**	**Third V_{gs} dependent parameter for impact ionization current**
S_{iid}	**siid**	**V_{ds} dependent parameter of drain saturation voltage for impact ionization current**
a_{gidl}	**Agidl**	**GIDL constant**
b_{gidl}	**Bgidl**	**GIDL exponential coefficient**
c	**Ngidl**	**GIDL V_{ds} enhancement coefficient**
n_{tun}	**Ntun**	**Reverse tunneling non-ideality factor**
n_{diode}	**Ndiode**	**Diode non-ideality factor**
n_{recf0}	**Nrecf0**	**Recombination non-ideality factor at forward bias**
n_{recr0}	**Nrecr0**	**Recombination non-ideality factor at reversed bias**
i_{sbjt}	**Isbjt**	**BJT injection saturation current**
i_{sdif}	**Isdif**	**Body to source/drain injection saturation current**
i_{srec}	**Isrec**	**Recombination in depletion saturation current**
i_{stun}	**Istun**	**Reverse tunneling saturation current**
V_{rec0}	**Vrec0**	**Voltage dependent parameter for recombination current**

V_{tun0}	**Vtun0**	**Voltage dependent parameter for tunneling current**
N_{bjt}	**Nbjt**	**Power coefficient of channel length dependency for bipolar current**
L_{bjt0}	**Lbjt0**	**Reference channel length for bipolar current**
V_{abjt}	**Vabjt**	**Early voltage for bipolar current**
A_{ely}	**Aely**	**Channel length dependency of early voltage for bipolar current**
A_{hli}	**Ahli**	**High level injection parameter for bipolar current**

E.2. AC and Capacitance Parameters

Symbol used in equation	Symbol used in SPICE	Description
V_{sdfb}	**vsdfb**	**Source/drain bottom diffusion capacitance flatband voltage**
V_{sdth}	**vsdth**	**Source/drain bottom diffusion capacitance threshold voltage**
DelVt	**delvt**	**Threshold voltage adjust for C-V**
acde	**acde**	**Exponential coefficient for charge thickness in capMod=3 for accumulation and depletion regions.**
moin	**moin**	**Coefficient for the gate-bias dependent surface potential.**