Josephson Logic Scaling: Issues and Countermeasures

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- JJ technology for computers: Really?
- Scalability disadvantage, what to do about it?
- Important new old concept to be revisited.

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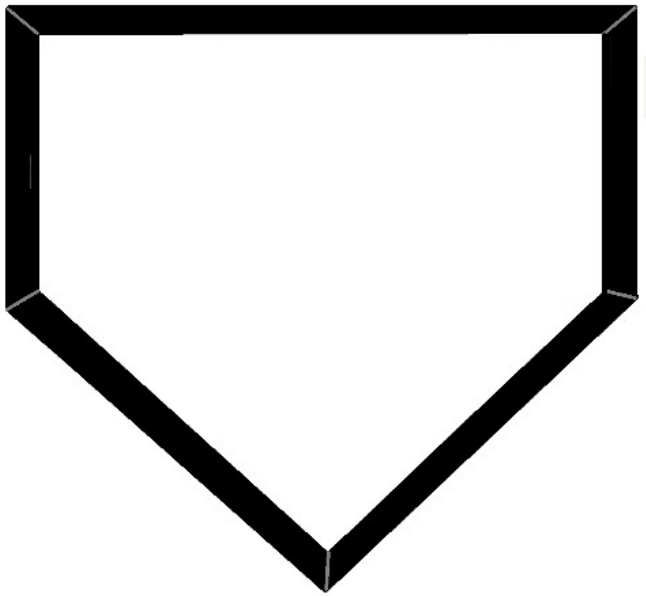
Three Strikes, and ...

1. Two-terminal limitations (70%)
2. Requires inductors, magnetic sensitivity issues (20%)
3. 4K operation (10%)

Coefficient of awfulness



As things now stand, You're Out!

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What Now?

In this talk, I will:

1. Explain Strikes 1 and 2 in more detail.

2. Reveal how to **eliminate Strike 2**, and Discuss ways of fighting Strike 1.

Two-Terminal Device Issues

A Josephson junction, like an Esaki tunnel diode,
Is a threshold switch.

CMOS

Variable: Vth (Threshold Voltage)

Static effect of variation: none

Result of 10% variation:
100M transistors on chip routinely

JJ

Variable: Ic (Critical Current)

Static effect of variation:
Kirchhoff's Law, Ic + Iin + Iout = 0

Result of 10% variation:
No yield at single-digit gate count.

True for ALL JJ logic families!

Countermeasures

1. Improve process uniformity. One can only go so far, will affect circuit size – large size required for uniformity.

2. Accept the limitation, use lots of chips.

3. Invent a three-dimensional epitaxial junction, that is atomically reproducible and provides exact Ic matching. (Buckyball?)

4. Hybridize with with another technology that provides isolation, amplification, etc.
   a. Fine-grained hybridization: JJ/semiconductor on same chip
   b. Coarse-grained hybridization: separate chips TSV (through-substrate via) packaging.

   TSV is important!

5. Other ideas?

Related Issues for SFQ

Highly constraining interconnection limitations

Fan-in and fan-out always one – additional inputs/outputs require added gates or splitters.

Long runs require either JTL or PTL.

Not a show stopper but a major nuisance impacting:

1. Feasibility of logic synthesis and auto place and route, currently unavailable.

2. JJ count adds up quickly, limiting capability per chip.

Countermeasures

1. Restrict applications to those with strong locality, such As pipelines. I.e., do everything with shift registers!

2. Hybridization? Use another technology (CMOS?) As “glue” between JJ blocks.

Inductors are Evil

1. They couple to each other and to everything else in the universe.

2. The inductance value is difficult to control, and sometimes to predict.

3. They don't scale to small dimensions easily.

4. They make the circuit extraordinarily sensitive to magnetic fields (SQUID loops).
   a. Careful magnetic shielding of the JJ chips required.
   b. How to shield from high-current supply lines?
   c. Sensitivity to trapped flux, requiring moats, etc.

5. Did I mention that inductors are evil?

Inductorless SFQ!

In RSFQ and family, any inductor that is not a transformer can be replaced by a current-to-phase transducer.

How to implement a current-to-phase transducer?
Use Josephson junctions!

Assertion: Any RSFQ gate can be implemented with these components:

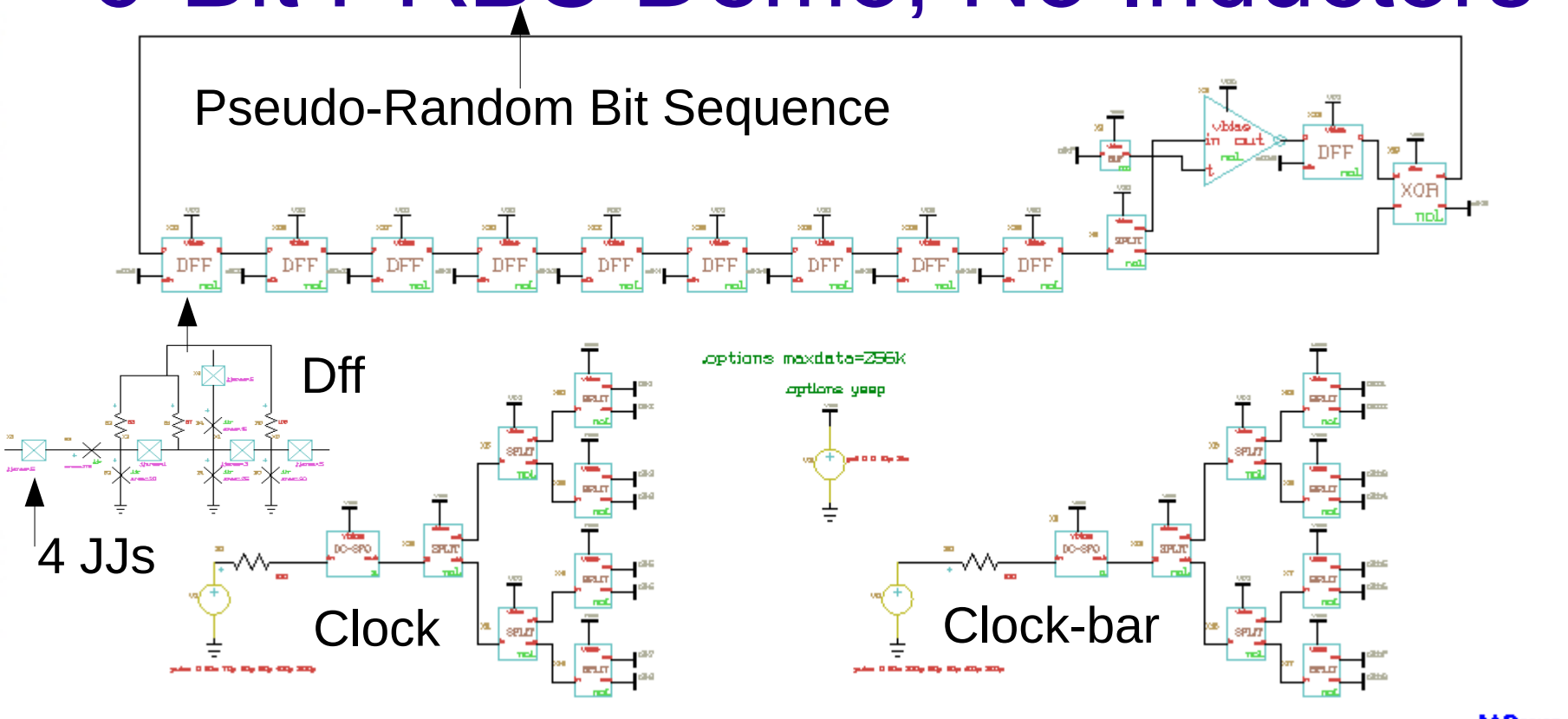
a. Josephson junctions that pulse.
b. Stacks of four Josephson junctions that act like inductors and never pulse. Why four? Good compromise for requirements.

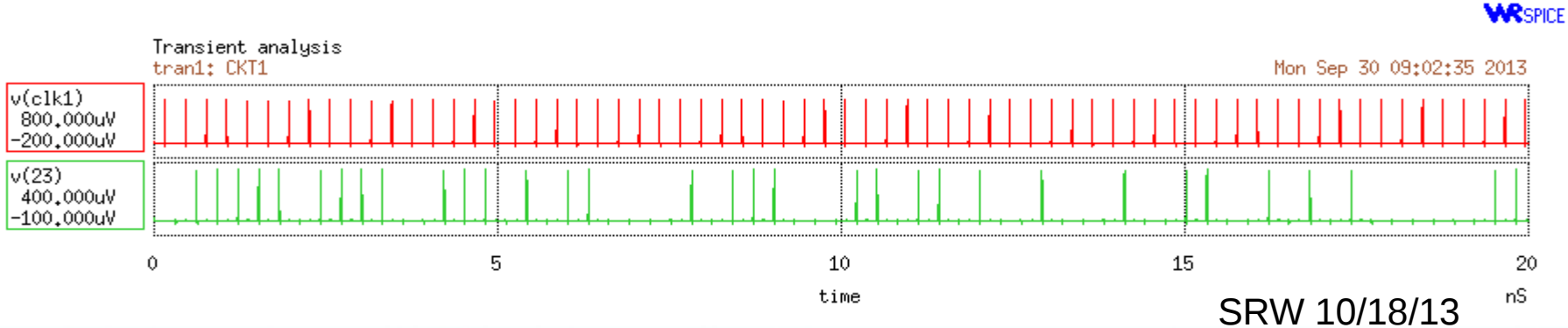
Stacks? Yes, must be vertical or too much parasitic inductance.

Process Development

1. Fabrication of four-junction equal-Jc in-situ “trilayers”.
2. Ability to pattern into four junctions and contact top and bottom.
3. Ability to remove or short out three of the junctions, providing a single junction.
4. Probably should integrate with planarized metal stack, as junction stack will be thick.

6-Bit PRBS Demo, No Inductors





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Inductorless SFQ Benefits

1. Circuits can have arbitrarily small area, limited by junction size and wiring.

2. Far lower magnetic sensitivity.
   a. Much less, or possibly no shielding required.
   b. Much less worry about trapped flux, can possibly avoid moats.

3. May help with Strike 1. Consider the Ic•L product:
   Ic•L = Ic•(ħ/(2e•Ic•cos(φ)) Ic cancels!

If critical currents track, Ic drops out, meaning (I think) that the circuits are less sensitive to Ic variation. This requires More study!

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Thoughts on Where to Go

1. Develop the 4/1 junction technology, probably in conjunction with planarization technology.

2. Very seriously address hybridization approach.
   a. Revisit the applications that were important in the 80s/90s when life was good in this field. We DO have memory, NOW. This should change everything!
   b. Consider ULP cryo-cmos, superconductivity/JJs must fit Somewhere (?).

3. Develop TSV for JJ chips.
   a. Can the metal be superconducting? Does it need to be?
   b. 3-D is the only way that the raw speed of RSFQ can be realized at sub-system level (Bedard, 1cm cube).

Ultra-Low Power Cryo-CMOS

Development path for CMOS, requires

a. improved threshold voltage control.
b. reduced gate oxide thickness (high transconductance).
c. increased doping (lower resistance).
d. operation at cryo temperature, ONLY.

Objective: lower Vdd operation. Vdd can track Vt for noise.

Payoff: Refrigeration penalty is 1/T, CMOS power dissipation goes as Vdd squared. Total computer power proportional to temperature!

The next Moore's law? (T → T/2 every 18 months)
Where does superconductivity fit?

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